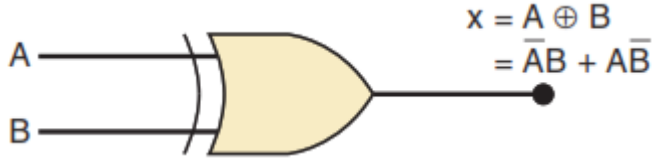
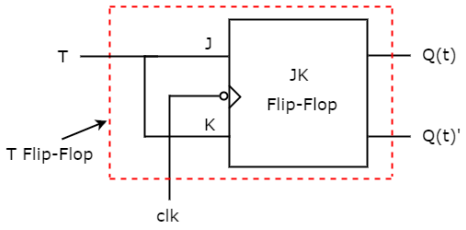
Important suggestions to examiners:

1) The answers should be examined by key words and not as word-to-word as given in the model answer scheme.
2) The model answer and the answer written by candidate may vary but the examiner may try to assess the understanding level of the candidate.
3) The language errors such as grammatical, spelling errors should not be given more importance. (Not applicable for subject English and communication skills)
4) While assessing figures, examiner may give credit for principle components indicated in a figure. The figures drawn by candidate and model answer may vary. The examiner may give credit for any equivalent figure drawn.
5) Credits may be given step wise for numerical problems. In some cases, the assumed constant values may vary and there may be some difference in the candidate's answers and model answer.
6) In case some questions credit may be given by judgment on part of examiner of relevant answer based on candidate understands.
7) For programming language papers, credit may be given to any other program based on equivalent concept.

Q.1	**Attempt any FIVE of the following**	**10 Marks**
a)	**Sketch symbol and write truth table of two input EX-OR gate.**	
Ans:	1 mark for diagram and 1 for TT  A B x 0 0 0 0 1 1 1 0 1 1 1 0	
b)	**Define the term 'Multiplexer'. State two examples of multiplexer.**	
Ans:	1 mark for definition and 1 for types A digital multiplexer or data selector is a logic circuit that accepts several (many) digital data inputs and selects one of them at any given time to pass on to the output. 1. Two input multiplexer 2. Four input multiplexer 3. Eight input multiplexer	
c)	**Implement T flip flop using J K flip flop. Write its truth table.**	
Ans:		

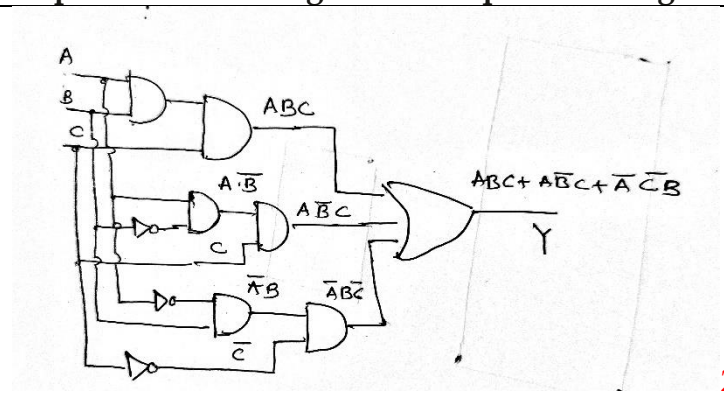
1 mark for Truth table and 1 for diagram

T flip-flop input	Present State	Next State
T	Qt	Qt+1
0	0	0
0	1	1
1	0	1
1	1	0



d) Implement following Boolean equation using fundamental gates :Y=ABC+A$\overline{B}$C+ $\overline{A}$ $\overline{C}$B

Ans:



2 marks for correct diagram

e) Identify direct addressing instructions from following instructions :
(i) MOV RO, R5 (ii) MOV RO, 80 H (iii) MOV RO, #75H (iv) ADD A, 45 H

Ans: Instructions ii) and iv) are direct addressing as 80H and 45H are direct addresses 2marks

f) If initial content of accumulator is 44 H, find out the new content of accumulator after execution of the instruction RR A

Ans: Contents of Acc will be 22H (as RR A divides acc by 2) 2 marks

g) Find out number of data lines required to interface 16 LEDs arrange in the 4 x 4 matrix form.

Ans: 4+4=8, eight lines are required for 4x4 matrix of 16 LEDs 2 marks

Q. 2 Attempt any THREE of the following 12 Marks

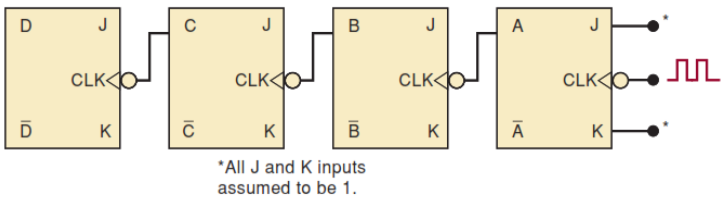
a) Define following terms related to logic families :
(i) Noise Margin (ii) FAN-OUT (iii) Propagation delay (iv) Power dissipation

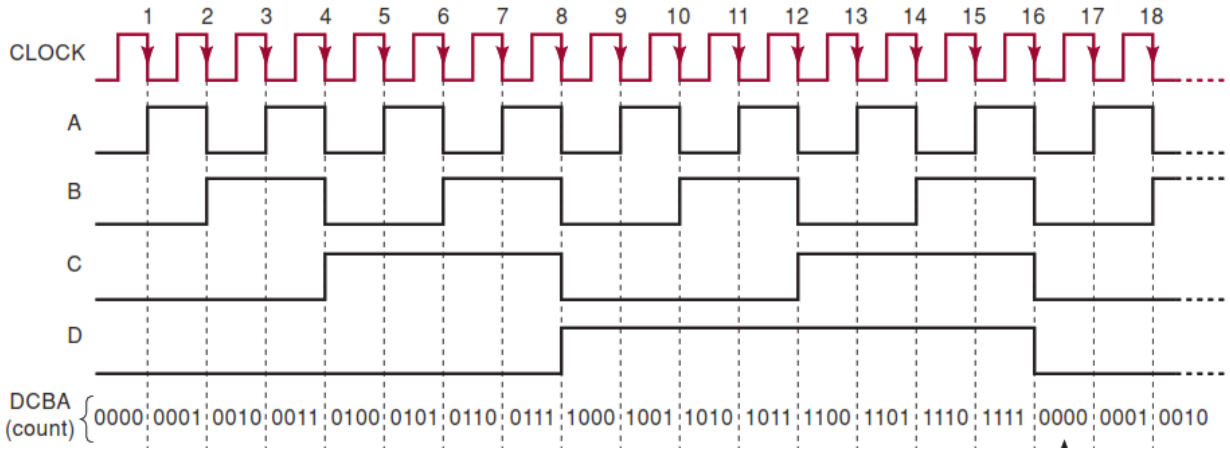
Ans: 1 marks for each definition

i) Noise immunity is measured in terms of **noise margin**.

High state Noise margin = $V_{NH} = V_{OH(min)} - V_{IH(min)}$

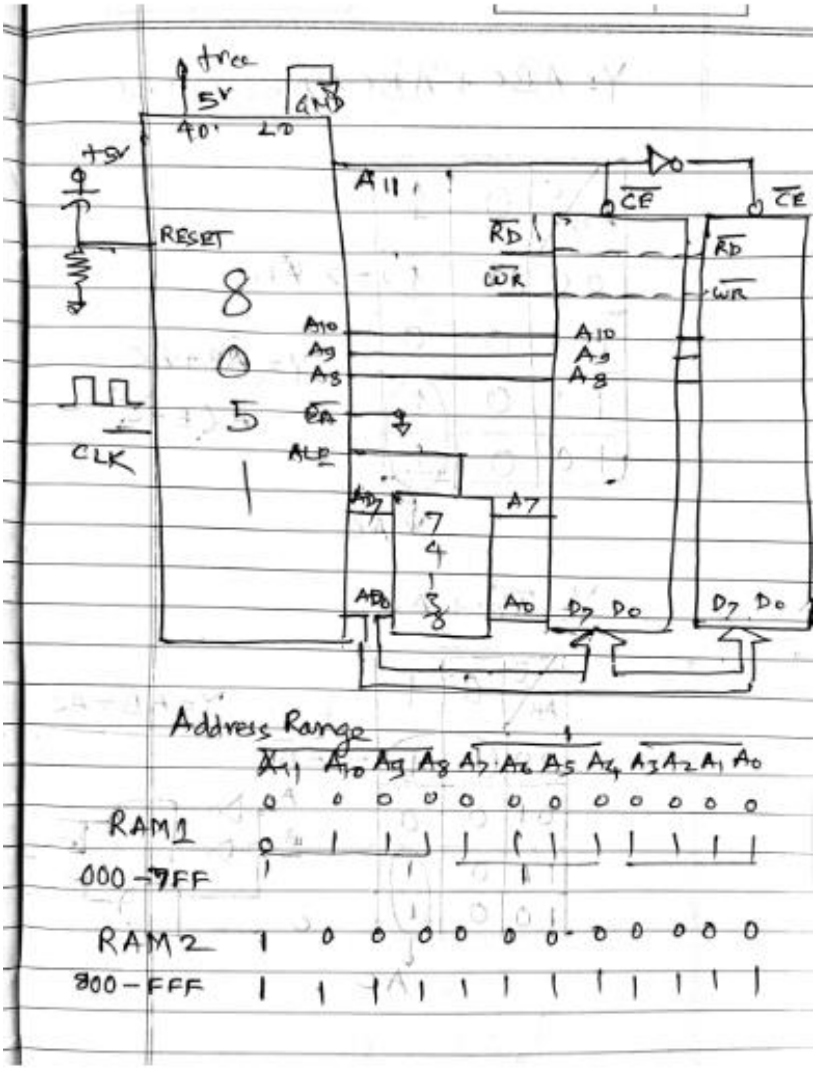
Low state Noise margin = $V_{NL} = V_{IL(max)} - V_{OL(max)}$

	i) The f**an-out** is defined as the maximum number of logic inputs that an output can Drive reliably. ii) Propagation delay is defined as t_{PLH} Delay time in going from logical 0 to logical 1 state (LOW to HIGH) t_{PHL} Delay time in going from logical 1 to logical 0 state (HIGH to LOW) iii) Average power dissipation is defined as $PD_{(avg)} = ICC_{(avg)} * V_{CC}$
b)	**State Demorgan's theorem's and prove both theorems using truth table.**
Ans:	2 marks for statement and 2 marks for equation **De Morgan's 1st theorem** states that when the OR sum of two variables is inverted, this is the same as inverting each variable individually and then ANDing these inverted variables. **De Morgan's 2nd theorem** says that when the AND product of two variables is inverted, this is the same as inverting each variable individually and then ORing them. In Boolean equation form it can be written as $\overline{(x + y)} = \bar{x} \cdot \bar{y}$ $\overline{(x \cdot y)} = \bar{x} + \bar{y}$
c)	**State functions of preset, clear, clock and SR inputs related to SR flip flop.**
Ans:	1 mark each for each function **Preset Input**: is an asynchronous input to set the Q output to 1 **Clear Input:** is also asynchronous input to reset the Q output to 0 **Clock Input:** is used to input external logic clock pulse (HIGH-LO) to the flip-flop. Depending upon the status of the input signal Q output changes on each clock pulse transition (Lo-Hi, Hi-Lo) **SR input:** The S input is Set input that is used to set the Q output. And R is the reset input which is used to reset Q output of the flipflop.
d)	**Sketch diagram of 4 bit asynchronous counter using suitable flip flop. Sketch timing diagram.**
Ans:	2 marks for diagram and 2 for timing diagram  *All J and K inputs assumed to be 1.



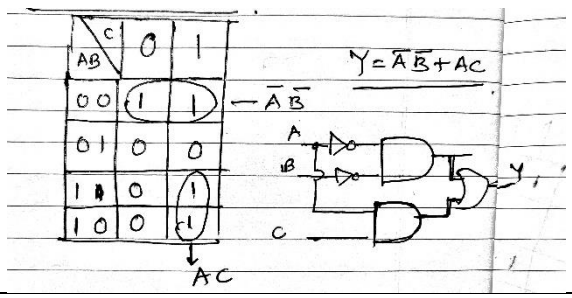
Q.3	**Attempt any THREE of the following** **12 Marks**
a)	**List out any four assembler directives and state their functions.**
Ans:	**1 marks for each directive** **ORG directive:** It is used to specify starting address of the Program. A 16bit address follows ORG ORG 0020H will start program from 0020H memory location. **END directive:** It indicates end of the assembly language program **DB directive:** he DB directive is the most widely used data directive in the assembler. It is used to define the 8-bit data. When DB is used to define data, the numbers can be in decimal, binary, hex, or ASCII formats. **EQU directive:** This is used to define a constant without occupying a memory location. The EQU directive does not set aside storage for a data item but associates a constant value with a data label so that when the label appears in the program, itp constant value will be substituted for the label.
b)	**Sketch diagram showing interfacing of two chips of RAM having size 2k x 8 to 8051 microcontroller. Write its memory map.**
Ans:	

3 marks for diagram and 1 mark for address range



c) **Minimize following Boolean equation using `K' map : Y =$A\ \overline{B}\ C\ +\ \overline{A}\ \overline{B}\ C +\ \overline{A}\ \overline{B}\ \overline{C}\ +\ ABC$ and implement using basic gates.**

Ans: 2 mark for k map 2 mark for diagram



d) **List out three types of buses. State their functions.**

	1 for address bus 1 for data bus and 2 for control bus
Ans:	**1. Address Bus:** It is a group of lines which carry binary address of the peripheral to be interface. **2. Data Bus:** It is used to Read/Write to between CPU and the peripheral **3. Control Bus:** This is a group of lines that generates control signals e.g. RD, WR, CLOCKOUT etc.
Q.4	**Attempt any THREE of the following** **12 Marks**
a)	**List out features of any four addressing modes of 8051.**

Ans:	1.5 marks for each address modes
	1.**Immediate addressing mode:** In this Immediate Addressing Mode, the data is provided in the instruction itself. The data is provided immediately after the opcode. These are some examples of Immediate Addressing Mode.
	MOVA, #0AFH;
	2. **Register addressing mode:** In the register addressing mode the source or destination data should be present in a register (R0 to R7). These are some examples of RegisterAddressing Mode.
	MOVA, R5;
	MOVR0, A;
	3. Direct Addressing Mode: In the Direct Addressing Mode, the source or destination address is specified by using 8-bit data in the instruction. Only the internal data memory can be used in this mode. Here some of the examples of direct Addressing Mode.
	MOV80H, R6;
	MOVR2, 45H;
	MOVR0, 05H;
	4. **Register indirect addressing Mode:** In this mode, the source or destination address is given in the register. By using register indirect addressing mode, the internal or external addresses can be accessed. The R0 and R1 are used for 8-bit addresses, and DPTR is used for 16-bit addresses, no other registers can be used for addressing purposes. Let us see some examples of this mode.
	MOV 0E5H, @R0
	MOV @R1, 80H

b)	**With the help of PCON register, explain Power down mode and Idle mode of 8051.**
Ans:	2 marks for PCON format and 2 marks for explanation The format for PCON register is as follows  **Bit 7 – SMOD** **1 =** Baud rate is doubled in UART mode 1, 2 and 3. **0 =** No effect on Baud rate.

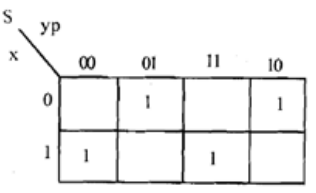
Bit 3:2 – GF1 & GF0:
These are general purpose bit for user.
Bit 1 – PD: Power Down
1 = Enable Power Down mode. In this mode, Oscillator clock turned OFF and both CPU and peripherals clock stopped. Hardware reset can cancel this mode.
0 = Disable Power down mode.
Bit 0 – IDL: Idle
1 = Enable Idle mode. CPU clock turned off whereas internal peripheral module such as timer, serial port, interrupts works normally. Interrupt and H/W reset can cancel this mode.
0 = Disable Idle mode.
Power down and Idle mode features are used to save power in microcontrollers. 8051 has inbuilt power saving feature which is useful in embedded applications where power consumption is main constraint. In **Power Down** mode, the oscillator clock provided to system is OFF i.e. CPU and peripherals clock remains inactive in this mode.
In **Idle** Mode, only the clock provided to CPU gets deactivated , whereas peripherals clock will remain active in this mode.
Hence power saved in power down mode is more than in idle mode.

c) Construct full adder circuit using K map.

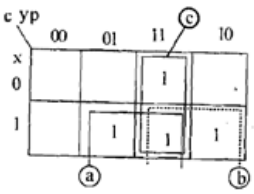
Ans: 2 marks for k map, 2 marks for description, 2marks for diagram

Inputs			Carry	Sum
x	y	p	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

(a) Truth table



(b) K-Map for 'S'



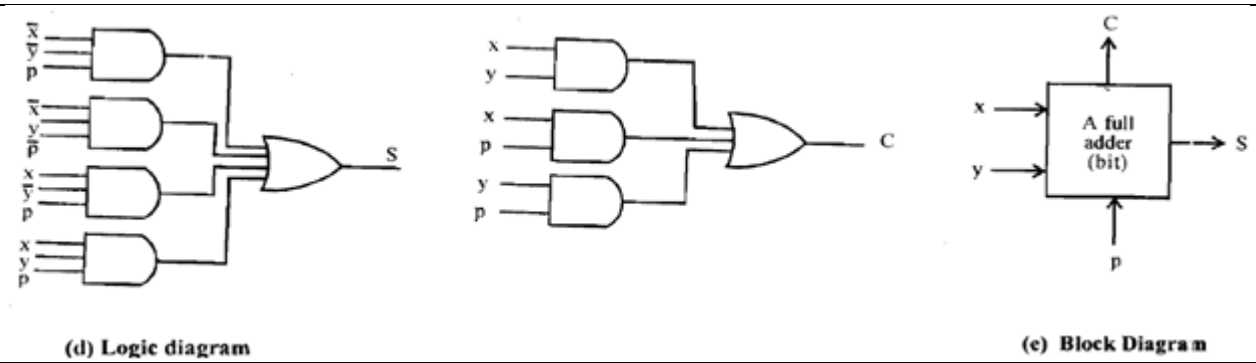
(c) K – Maps for 'C'

There are three inputs to full adder x,y and previous carry bit p. The truth table shows the all possible combinations and the results of addition Sum (s)and Carry (c). the K-map for both sum and carry are shown on right. The Boolean equations are as follows

$C = x\bar{p} + x\,y + \bar{y}\,p$

$S = \bar{x}\bar{y}\,p + \bar{x}yp^{-} + xy\bar{p} + x\,y\,p$

The logic circuit is shown in following diagram

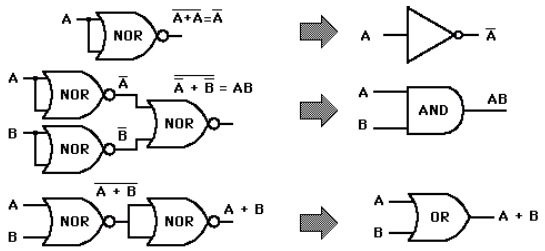


(d) Logic diagram (e) Block Diagram

d) Justify 'NOR gate is called as universal gate'. Sketch relevant diagram.

Ans: 2 marks for explanation and 4 marks for diagram

NOR gate is universal gate which means that NOR gate can be used to construct any of the basic logic gates which is shown in the following diagram. From which it is clear that NOR gate is called as universal gate.



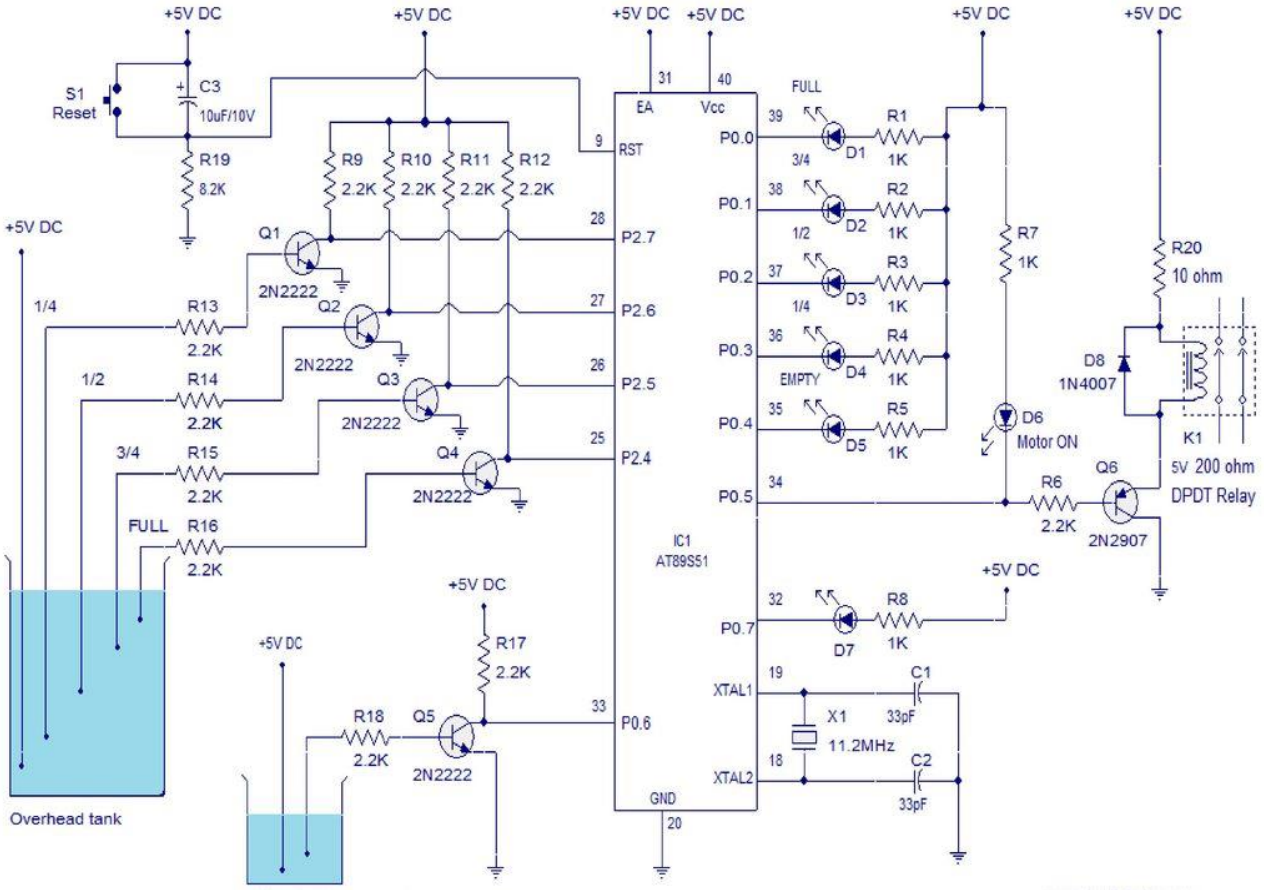
e) Compare microprocessor with microcontroller on the basis of any four factors.

Ans: 1.5 marks for each comparison

	Microprocessors	Microcontrollers
1	It is only a general purpose computer CPU	It is a micro computer itself
2	Memory, I/O ports, timers, interrupts are not available inside the chip	All are integrated inside the microcontroller chip
3	This must have many additional digital components to perform its operation	Can function as a micro computer without any additional components.
4	Systems become bulkier and expensive.	Make the system simple, economic and compact
5	Not capable for handling Boolean functions	Handling Boolean functions
6	Higher accessing time required	Low accessing time
7	Very few pins are programmable	Most of the pins are programmable
8	Very few number of bit handling instructions	Many bit handling instructions
9	Widely Used in modern PC and laptops	widely in small control systems
E.g.	INTEL 8086,INTEL Pentium series	INTEL8051,89960,PIC16F877

Q.5	**Attempt any TWO of the following**	**12 Marks**
a)	**Explain with neat diagram microcontroller based water level controller.** 4 marks for diagram and 2 marks for explanation	

Ans:



This water level controller monitors the level of the over head tank and automatically switches on the water pump when ever the level goes below a preset limit. The level of the over head tank is indicated using 5 leds and the pump is switched of when the over head tank is filled. The pump is not allowed to start if the water level in the sump tank is low and also the pump is switched off when the level inside the sump tank goes low during a pumping cycle. The circuit diagram of the water level controller is shown below.

The level sensor probes for the overhead tank are interfaced to the port 2 of the microcontroller through transistors. Have a look at the sensor probe arrangement for the overhead tank in Figure. A positive voltage supply probe goes to the down bottom of the tank. The probes for sensing 1/4, 1/2, 3/4 and FULL levels are placed with equal spacing one by one above the bottom positive probe. Consider the topmost (full level) probe, its other end is connected to the base of transistor Q4 through resistor R16. Whenever water rises to the full level current flows into the base of transistor Q4 which makes it ON and so its collector voltage goes low. The collector of Q4 is connected to P2.4 and a low voltage at P2.4 means the over head tank is not FULL. When water level goes below the full level probe, the base of Q2 becomes open making it OFF. Now its collector voltage

goes high and high at P2.4 means the tank is not full. The same applies to other sensor probes (3/4, 1/2, 1/4) and the microprocessor understands the current level by scanning the port pins P2.4 ,P2.5, P2.6 and P2.7. All these port pin are high (all sensor probes are open) means the tank is empty.
Port pin P0.5 is used to control the pump. When ever it is required start pumping, the controller makes P0.5 low which makes transistor Q6 ON which in turn activates the relay K1 that switches the pump. Also the LED d6 glows indicating the motor is ON. LED D7 is the low sump indicator. When the water level in the sump tank goes low, the controller makes P0.7 low which makes LED D7 to glow.

```
        MOV P2,#11111111B // initiates P2 as sensor input
        MOV P0,#11111111B // initiates P2 as the output port
        MOV A,#00000000B
MAIN:ACALL SMPCK // checks the level of the sump tank
          MOV A,P2 // moves the current status of P2 tp A
          CJNE A,#11110000B,LABEL1 // checks whether tank is full
          SETB P0.1
          SETB P0.2
          SETB P0.3
          SETB P0.4
          CLR P0.0 // glows full level LED
          SETB P0.5
LABEL1: MOV A,P2
          CJNE A,#01110000B,LABEL2 // checks whether tank is 3/4
          SETB P0.0
          SETB P0.2
          SETB P0.3
          SETB P0.4
          CLR P0.1 // glows 3/4 level LED
LABEL2: MOV A,P2
          CJNE A,#00110000B,LABEL3 // checks whether tank is 1/2
          SETB P0.0
          SETB P0.1
          SETB P0.3
          SETB P0.4
          CLR P0.2 // glows 1/2 level LED
LABEL3:MOV A,P2
          CJNE A,#00010000B,LABEL4 // checks whether tank is 1/4
```

```
        SETB P0.0
        SETB P0.1
        SETB P0.2
        SETB P0.4
        CLR P0.3 // glows 1/4 level LED
        JB P0.6, LABEL4
        CLR P0.5 // switches motor ON
LABEL4: MOV A,P2
        CJNE A,#00000000B, MAIN // checks whether tank is empty
        SETB P0.0
        SETB P0.1
        SETB P0.2
        SETB P0.3
        CLR P0.4 // glows EMPTY LED
        JB P0.6, MAIN // checks whether sump is low
        CLR P0.5 // switches motor ON
        SJMP MAIN
        SMPCK:JB P0.6,LABEL5 // checks whether sump is low
        SETB P0.7 // extinguishes the sump low indicator LED
        SJMP LABEL6
LABEL5: SETB P0.5 // switches the pump OFF
        CLR P0.7 // glows sump low indicator LED
LABEL6: RET
        END
```

b) **Develop ALP for 8051 to perform addition, anding, multiplication of two data — Data-1 is at memory location 55 H and Data 2 is 20 H. Store result at internal memory locations.**

Ans: 3 marks for addition program and 3 marks for multiplication

Assembly language program

;**Subtraction program**

```
        ORG 0000h
        SJMP MAIN
        ORG 0030H
        CLR C
MAIN:   MOV A,55H    ;LOA NO1 INTO ACC
        ADD A,20H    ;ADD TO NUMBER 2
        MOV 58H, A   ; STORE RESULT
```

```
                MOV A,#00H
                ADDC A,#00H  ; ADD CARRY
                MOV 59H,A
HERE:           SJMP HERE
                END
```

;MULTIPLICATION program

```
                ORG 0000h
                SJMP MAIN
                ORG 0030H
                CLR C
MAIN:           MOV A,55H    ;LOAD NO1 INTO ACC
                MOV 0F0H,A
                MOV A,20H  ;LOAD NO2 INTO 20H
                MUL AB
                MOV 58H, A    ; STORE RESULT
                MOV A,0F0H
                MOV 59H,A
HERE:           SJMP HERE
                END
```

c) Explain internal and external memory organization of 8051.

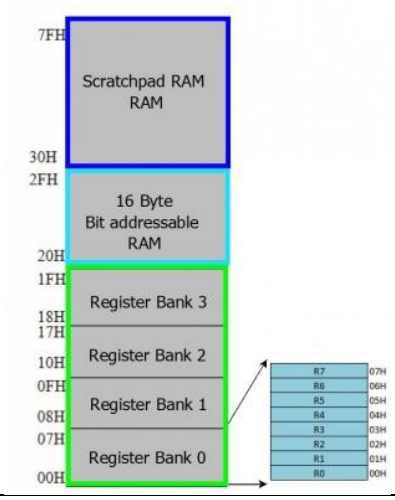
Ans: 3 marks for internal data and 3 marks for external program memory

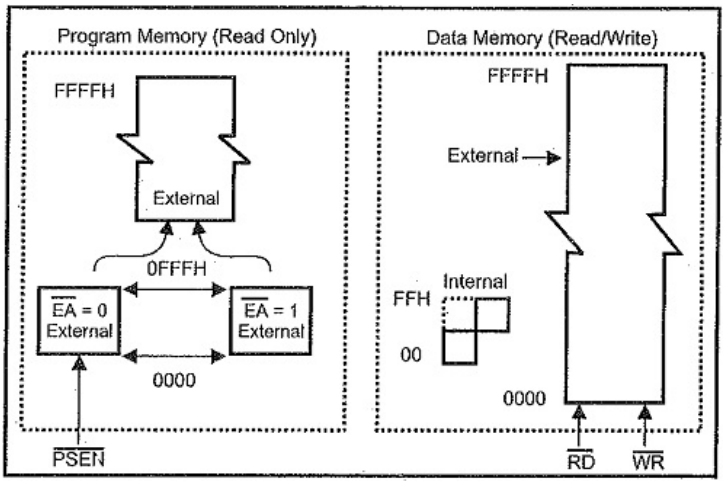
There are two types of memories for present day 8051 chips

a) Internal data memory
b) Internal program memory

The address range of internal data memory is 00h-7fh, SFRs i.e. special function registers are mapped within the address range 80-ffh and accessible be direct addressing. The internal program memory is 4kB and the address range is 000h-ffffh. The internal data memory 00h-7fh is divided into three sections Register Banks(00h-1fh,4 Banks each having 8 registers R0-R7), 128 bits bit addressable memory area(20h-2fh), scratch pad memory area (30h-7fh).

The internal program memory is mapped from 000h -fffh. Its accessible when /EA pin is at logic HI, External program memory/data memory can be connected to 8051 by using its bus structure. To access external program memory /EA to be kept at logic LO. The address range of external program memory is on 64K as there are 16 address lines. The data bus is of 8 bits.





Q.6 **Attempt any TWO of the following** **12 Marks**

a) **Explain functions of all pins of Port 0, Port 1, Port 2 and Port 3.**

Ans: **4 marks for P0-P2 and 2 marks for P3**

Port 0: It has two functions. It is used as lower order multiplexed address/data bus (AD0-AD7) and it is used as general purpose I/O port. It has open collector output, it needs pullup resistance to be connected externally.

Port 1: It is only used as general purpose I/O port and it has no other function

Port 2: It has two functions. It is used as higher order address bus A8-A15. It is also used as general purpose I/O port.

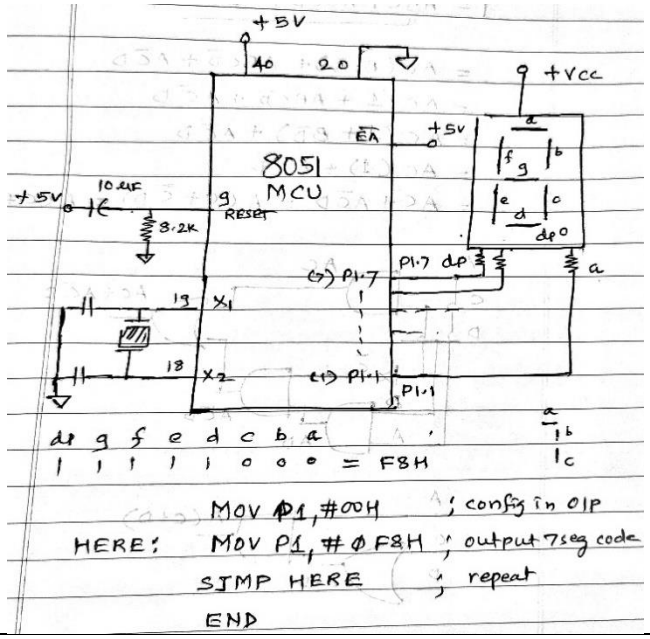
Port 3: Each pin of port 3 has a different function as shown in below table. Alternatively it can also be used as general purpose I/O port.

PORT 3 ALTERNATE FUNCTIONS :

P3 BIT	FUNCTION	PIN
P3.0	RXD	10
P3.1	TXD	11
P3.2	$\overline{INT0}$	12
P3.3	$\overline{INT1}$	13
P3.4	T0	14
P3.5	T1	15
P3.6	$\overline{WR}$	16
P3.7	$\overline{RD}$	17

b) **Sketch diagram showing interfacing of single 7-segment common Anode display to 8051. Develop ALP to display number '7; on it.**

Ans: 3 marks for diagram and 3 marks for program



c) **Convert following Boolean equation to standard SOP form and implement using NAND-NAND logic.**

(i) $y = A\,\overline{B}\,C + ABC\overline{D} + A\,\overline{C}\,D + ABC$ **ii)** $y = PQ + PQR + PQ\overline{R}$

Ans: 3 marks each

$$Y = A\overline{B}C + ABC\overline{D} + A\overline{C}D + ABC$$

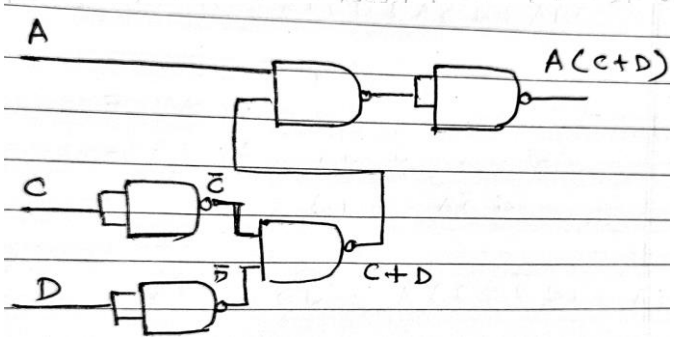
$$= AC(B+\overline{B}) + ABC\overline{D} + A\overline{C}D$$

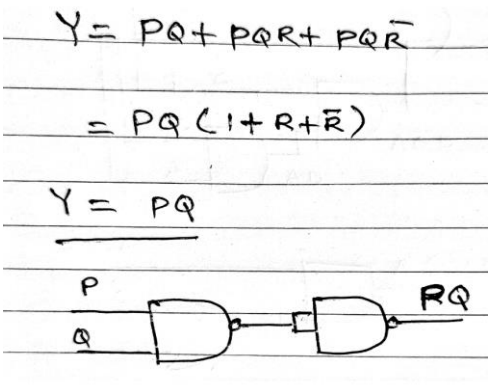
$$= AC \cdot 1 + ABC\overline{D} + A\overline{C}D$$

$$= AC(1 + B\overline{D}) + A\overline{C}D$$

$$= AC(1) + A\overline{C}D$$

$$= AC + A\overline{C}D = A(C + \overline{C}D) = A(C+D)$$



	ii) 

----------END----------