WINTER – 2022 EXAMINATION
Model Answer

Subject Name: Linear Integrated Circuits. **Subject Code:** 22423

Important Instructions to examiners:

1) The answers should be examined by key words and not as word-to-word as given in the model answer scheme.
2) The model answer and the answer written by candidate may vary but the examiner may try to assess the understanding level of the candidate.
3) The language errors such as grammatical, spelling errors should not be given more Importance (Not applicable for subject English and Communication Skills.
4) While assessing figures, examiner may give credit for principal components indicated in the figure. The figures drawn by candidate and model answer may vary. The examiner may give credit for any equivalent figure drawn.
5) Credits may be given step wise for numerical problems. In some cases, the assumed constant values may vary and there may be some difference in the candidate's answers and model answer.
6) In case of some questions credit may be given by judgement on part of examiner of relevant answer based on candidate's understanding.
7) For programming language papers, credit may be given to any other program based on equivalent concept.
8) As per the policy decision of Maharashtra State Government, teaching in English/Marathi and Bilingual (English + Marathi) medium is introduced at first year of AICTE diploma Programme from academic year 2021-2022. Hence if the students in first year (first and second semesters) write answers in Marathi or bilingual language (English +Marathi), the Examiner shall consider the same and assess the answer based on matching of concepts with model answer.

Q. N.	Sub Q.N.	Answer	Marking Scheme
1.		**Attempt any Five of the following**	**10 M**
	a)	**Define Input offset voltage and Input bias current.**	**2M**
	Ans	**Inputs offset voltage:** A small input voltage is required to be applied to an OpAmp in order to make its output zero called as Inputs offset voltage **Input bias current:** It is defined as the average of the currents flowing into the two input terminals of the OpAmp $Ib=\frac{Ib1+Ib2}{2}$	**1 Mark for each definition**
	b)	**Draw the circuit diagram of voltage follower.**	**2M**

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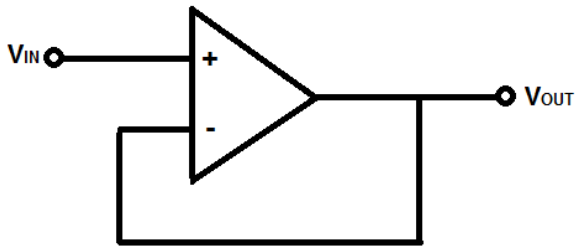
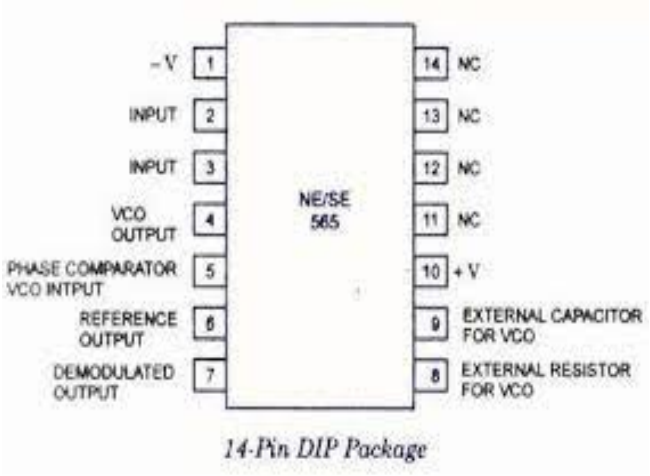
	Ans		2 Mark for correct diagram
	c)	**Draw pin diagram of IC 565.**	**2M**
	Ans	 *14-Pin DIP Package*	2 Mark for correct pin name
	d)	**Define cutoff frequency and passband.**	**2M**
	Ans	1) **Cutoff frequency:** It is the range of frequency over which stop band and pass band separated OR **Cutoff frequency:** The voltage gain at -3db frequency is 0.707 times or 70.7% of the maximum gain. 2) **Passband:** It is the band or range of frequencies which allowed to pass through to the output by the filter without any attenuation	1 Mark for each defination
	e)	**List two applications of IC LM324.**	**2M**
	Ans	LM324 is applicable for the 1. Oscillators 2. Amplifiers	1 Mark for each application

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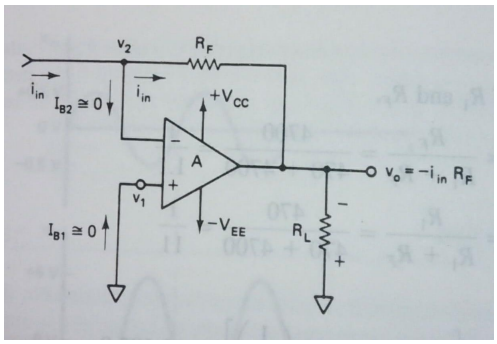
		3. Rectifiers 4. Comparators	(any two)
	f)	**Draw circuit diagram of I to V converter.**	**2M**
	Ans		2 Mark for correct diagram
	g)	**State two merits of active filters over passive filters.**	**2M**
	Ans	Merits 1) Flexibility in gain and frequency adjustment. 2)No loading problem 3) Low cost 4) No insertion loss 5) pass band gain 6) Small component size 7) Use of inductor can be avoided	1 Mark each merit (any two)
2.		**Attempt Any THREE of the following**	**12M**
	a)	**Describe the operation of PLL as FM demodulator.**	**4M**

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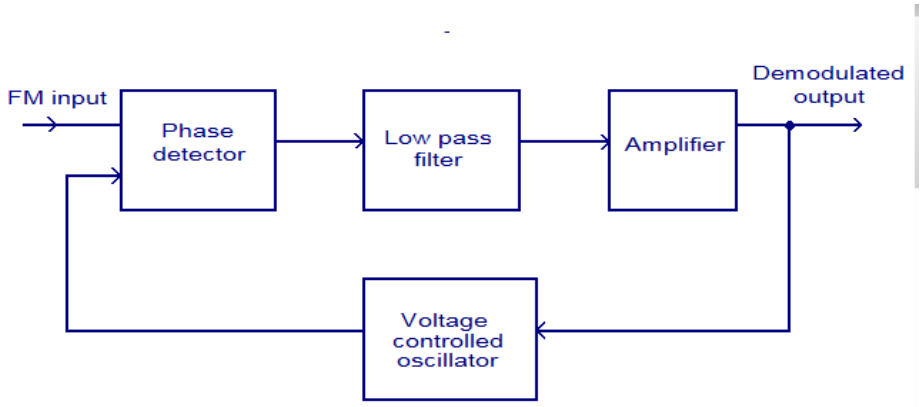
	Ans	 PLL FM demodulator circuit **Operation :** • The FM signal which is to be demodulated is applied at input of the PLL. • As the PLL is locked to the FM signal,the VCO starts tracking the instantaneous frequency in the FM input signal. • The error voltage produced at the output of the amplifier is proportional to the deviation of input frequency from the center frequency of FM.Thus the AC component of the error voltage represent the modulating signal.Thus at the error amplifier output we get demodulated output • The FM demodulator using PLL ensures a highly linear relationship,between the instantaneous input frequency and VCO control voltage (error amplifier output)	**2M for circuit diagram** **2M for operation**
	b)	**Sketch first order Butterworth low pass filter with component value at cutoff frequency of 15 kHz with passband gain of 2.**	**4M**
	Ans	Given: cutoff frequency (Fc) = 15 kHz passband gain = 2. Avf =2, fc= 15kHz $Avf = (1+R_F / R_1)$ $2 = (1+R_F / R_1)$ Thus , $R_F / R_1 = 1$ Assume $R_F = 10K\Omega$ **$R_F = R_1 = 10K\Omega$**	**1 M for Sketch** **1 M calculation of Rf and R1.** **1 M for calculation of R.**

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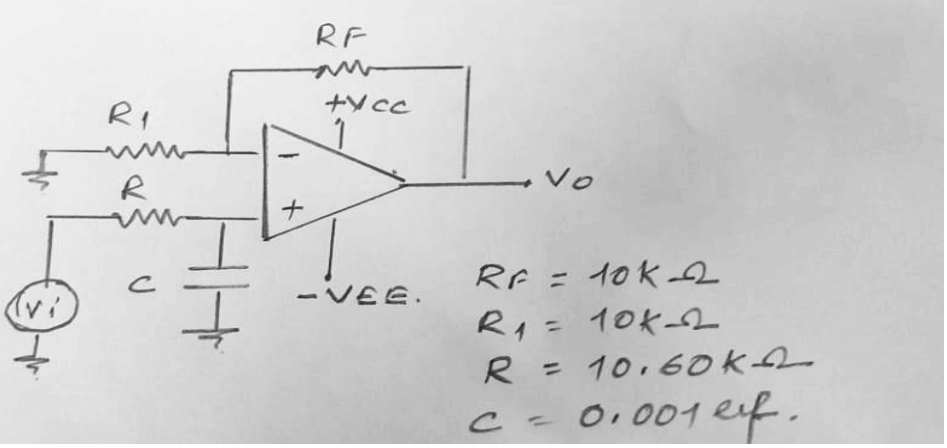
		Assume $C = 0.001\mu f$. But $f_c = \frac{1}{2\pi RC} = \frac{1}{2\pi \times R \times 0.001 \times 10^{-6}}$ $\therefore R = \frac{1}{2\pi \times 15 \times 10^{3} \times 0.001 \times 10^{-6}}$ $\therefore R = 10.60\,k\Omega$  $R_F = 10k\Omega$ $R_1 = 10k\Omega$ $R = 10.60k\Omega$ $C = 0.001\mu f$.	**1 M for calculation of C**
	c)	**In op-amp based Schmitt trigger, $R_2 = 200\Omega$, $R_1 = 50\Omega$, Vin = 500 mV_{pp} sinewave, saturation voltage = ± is v. Determine threshold Voltage V_{UTP} , V_{LTP}.**	**4M**
	Ans	$V_{UTP} = \frac{R_2}{(R_1+R_2)} \times (+V_{sat})$ $= \frac{200}{(50+200)} \times (+15)$ $= 0.8 \times (+15)$ $V_{UTP} = +12V$ $V_{LTP} = \frac{R_2}{(R_1+R_2)} \times (-V_{sat})$ $= \frac{200}{(50+200)} \times (-15)$ $= 0.8 \times (-15)$ $V_{LTP} = -12V$	2 Mark for UTP and 2Mark for LTP

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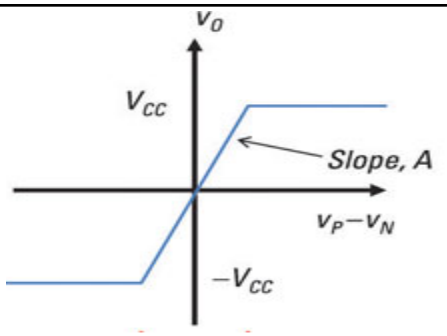
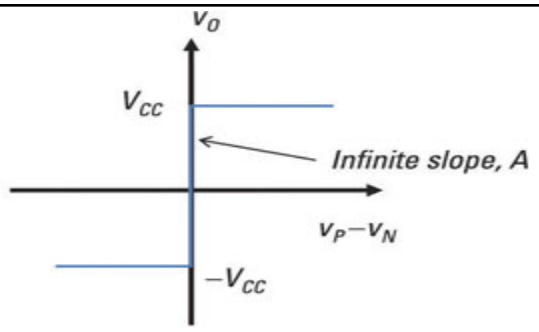
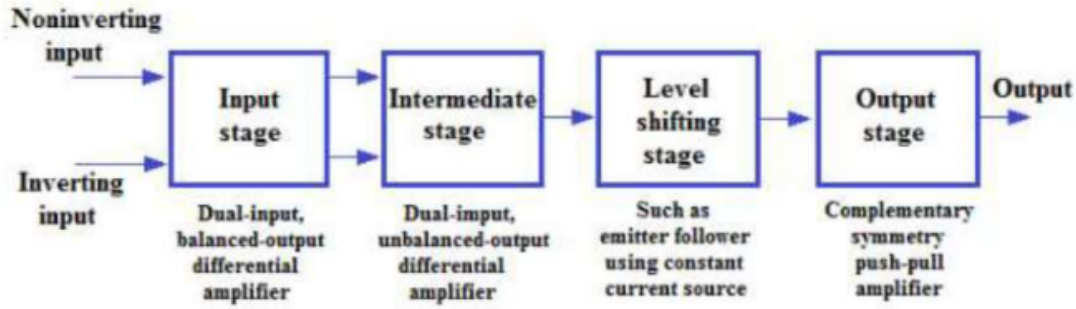
	d)	**Draw ideal and practical voltage transfer curve of op-amp.**	**4M**
	Ans	 **a)** **practical voltage transfer curve**  **b)** **Ideal voltage transfer curve**	**2 M each**
Q.3		**Attempt any THREE of the following.**	**12 M**
	a)	**Draw block diagram of OPAMP and state function of each block.**	**4M**
	Ans	 **Fig: Block diagram of OP- AMP** **Explanation:** **Input stage:** It is the dual input, balanced output differential amplifier. This stage generally provides most of the voltage gain of the amplifier and also establishes the input resistance of the op-amp. **Intermediate stage:** It is usually another differential amplifier, which is driven by the output of the first stage. In most amplifiers, the intermediate stage is dual input and unbalanced(single-ended) output. Because direct coupling is used, the dc voltage at the output of the intermediate stage as well above ground potential. **Level translator:** It is used after the intermediate stage to shift the dc level at the output of the intermediate stage downward to zero volts with respect to the ground. **Output stage:** The final output stage is usually a push-pull complementary amplifier output stage. The output stage increases the output voltage swing and raises the current-supplying capability of the op-amp.It also provides low output resistance.	**2M Block diagram, Explanation of 4 blocks 1/2 M each block**

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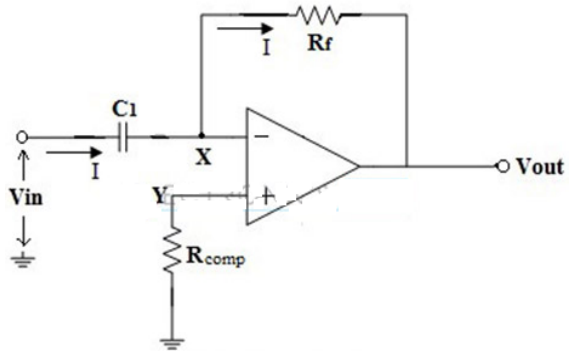
	b)	**Draw the circuit of basic differentiator and derive output expression**	**4M**
	Ans	**Circuit diagram of Differentiator:**  **Derivation of output expression :** When the input is a positive-going voltage, a current I flows into the capacitor C_1, as shown in the figure. Since the current flowing into the op-amp's internal circuit is zero, effectively all of the current "I "flows through the resistor R_f. The output voltage is, $$V_{out} = -(I * R_f)$$ Here, this output voltage is directly proportional to the rate of change of the input voltage. From the figure, node 'X' is virtually grounded and node 'Y' is also at ground potential i.e., $$V_X = V_Y = 0 .$$ From the input side, the current I can be given as: $$I = C_1 \{d(V_{in} - V_X) / dt\} = C_1 \{d(V_{in}) / dt\}$$ From the output side, the current I is given as: $$I = -\{(V_{out} - V_X) / R_f\} = -\{V_{out} / R_f\}$$ Equating the above two equations of current we get: $$C_1 \{d(V_{in}) / dt\} = -V_{out} / R_f$$ $$V_{out} = -C_1 R_f \{d(V_{in}) / dt\}$$ Above equation indicates that the output is $C_1 R_f$ times the differentiation of the input voltage. The product $C_1 R_f$ is called as the RC time constant of the differentiator circuit. The negative sign indicates the output is out of phase by 180^0 with respect to the input.	**Diagram 2M, Derivation 2M**
	c)	**Draw a neat circuit diagram of analog divider using log- antilog amplifiers and explain its operation.**	**4M**

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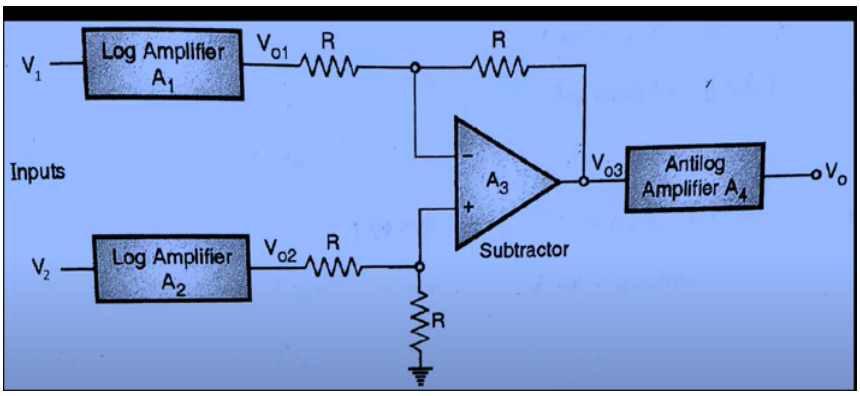
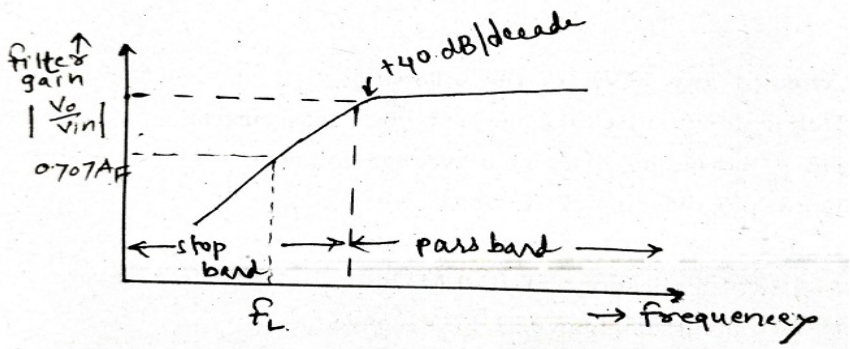
	Ans	**Analog divider using log-anti log amplifiers:**  **Explanation:** Analog Divider using log antilog amplifiers For Log amplifier :$V_O = -\eta V_T \log \frac{V_{in}}{I_O R}$ $V_{o1} = -\eta V_T \log \frac{V_1}{I_O R}$ $V_{o2} = -\eta V_T \log \frac{V_2}{I_O R}$ $\mathbf{V_{o3} = (V_{o2} - V_{o1})}$ $= (-\eta V_T \log \frac{V_2}{I_O R} + \eta V_T \log \frac{V_1}{I_O R})$ $= \eta V_T (\log \frac{V_1}{I_O R} - \log \frac{V_2}{I_O R})$ $= \eta V_T \log (\frac{V_1}{V_2})$ $V_O = -I_O R \text{ antilog } \frac{\eta V_T \log (\frac{V_1}{V_2})}{\eta V_T}$ $V_O = -I_O R \frac{V_1}{V_2}$ **Hence Vo ∝ V1/V2**	**Diagram 2M,** **Explanation 2M**
	d)	**Draw filter circuit for the following response. (Refer Fig.1)**  **Fig. No. 1**	**4M**

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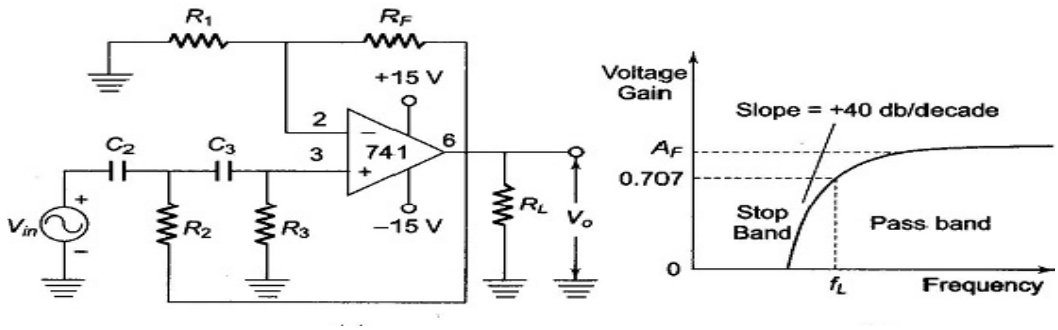
	Ans	**The response shown is of the second order high pass filter** Second order High pass filter circuit: 	**Identification of filter name 2M** **Diagram 2M**
Q.4		**Attempt Any THREE of the following**	**12M**
	a)	**Compare open loop and closed loop configuration.**	**4M**
	Ans		**Any 4 parameter 1M each**

Sr. No	Parameters	Open loop	Closed Loop
1	**Feedback**	No feedback is used.	Positive or negative feedback is used
2	**Input resistance**	Very high	Depends on the circuit
3	**Output resistance**	Low	Very low
4	**Bandwidth**	Bandwidth is low	Bandwidth is high
5	**Gain**	Voltage gain is very high	Voltage gain is low as compared to open loop
6	**Application**	Comparator ,zero crossing detector	It is used in linear amplifier, oscillator etc

	b)	**Explain the procedure to null the offset voltage with appropriate diagrams.**	**4M**

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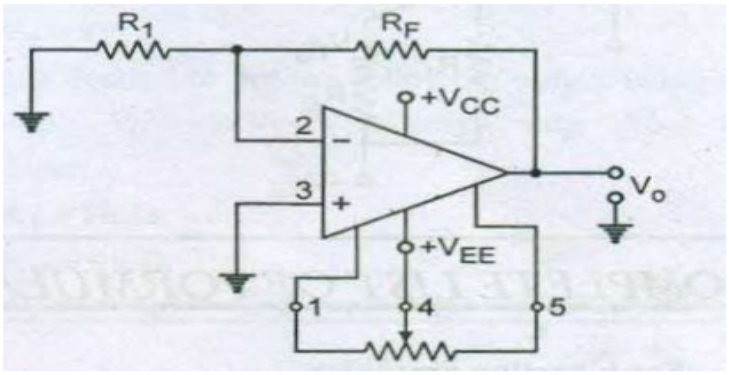
	Ans	 **Explanation:** 1) To make output voltage zero, input voltage should be zero, but we get minimum (less) output voltage called output offset voltage due to the presence of input offset at the input side. 2) This input offset voltage is present even when, both the input terminals are grounded . 3) Hence, a technique is used to make output offset voltage zero.This technique is called as offset nulling technique. In this technique, a 10 kΩ potentiometer is connected between the offset null pins of IC74I i.e. pin no. 1 and pin. 5 and the wiper of potentiometer is connected to pin no. 4 (i.e.-VEE). The wiper of the potentiometer is varied in such a way that input offset voltage becomes zero. Once input becomes zero, then output offset voltage also becomes zero. Thus, the op-amp is said to be nulled or balanced.	**Diagram 2M, Explanation 2M**
	c)	**Design the circuit to get the output voltage.** **$V_0 = 3V_1 + 2V_2$ where** **V_1 and V_2 are input voltages.**	**4M**

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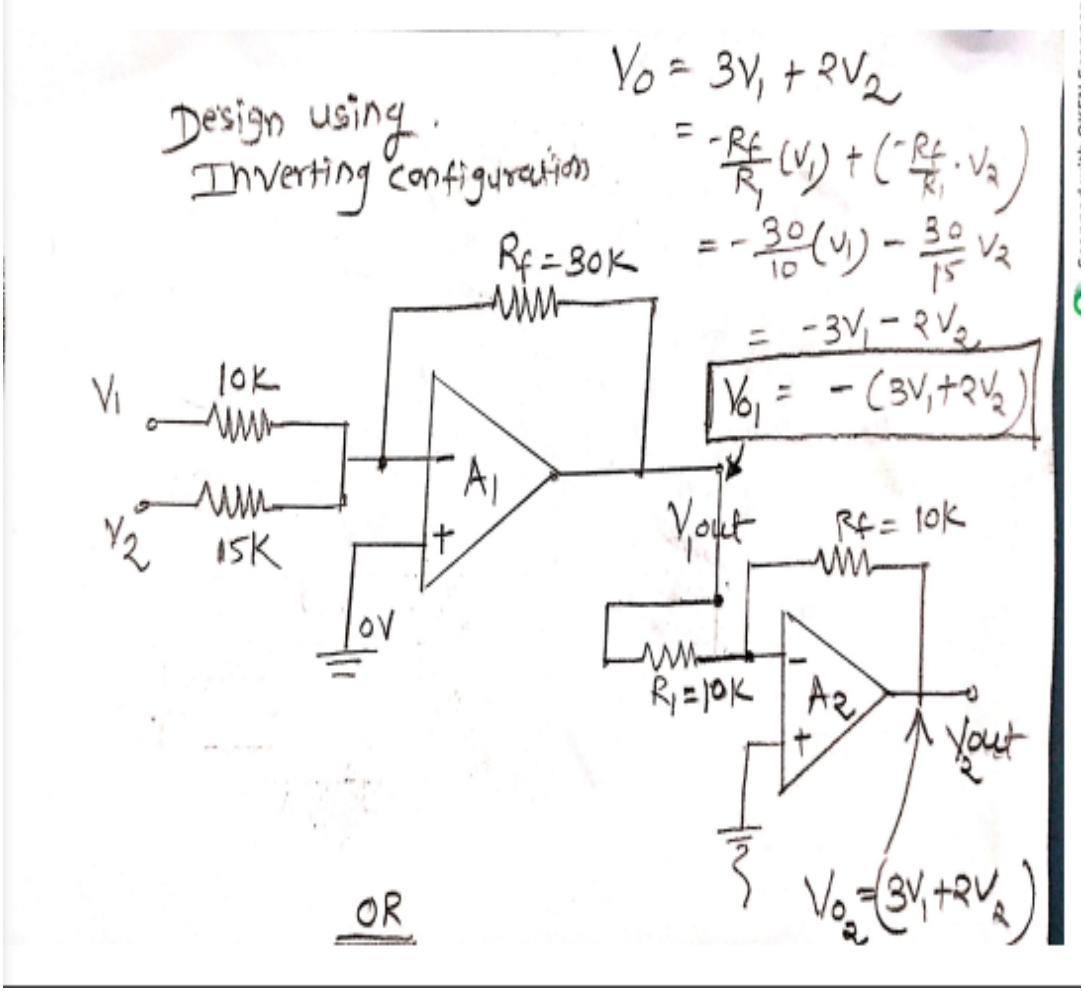
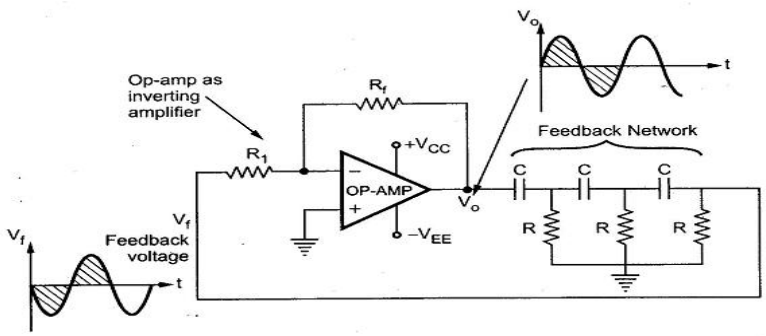
	Ans	 *Note: the values of R_F,R_1 & R_2 can be selected as any value to adjust gain ratio as given in the output equation.*	**4M**
	d)	**Explain phase shift oscillator using IC 741 with neat diagram.**	**4M**
	Ans	Circuit diagram: 	

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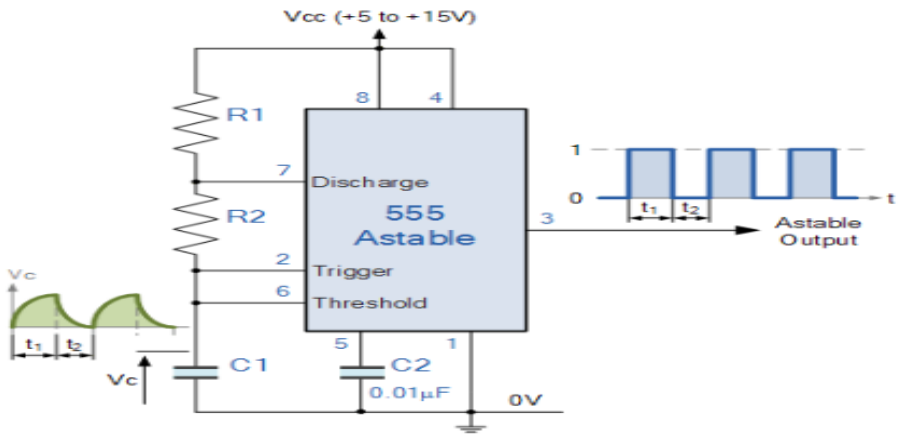
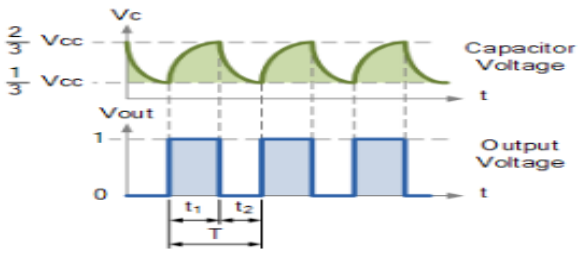
	Ans	**Explanation:** R-C phase shift oscillator using op-amp uses an op-amp in inverting amplifier mode. Thus it introduces the phase shift of 180° between input and output. The feedback network consists of 3-RC sections each producing 60° phase shift. Such an RC phase shift oscillator using op-amp is shown in Figure. The output of the amplifier is given to the feedback network. The output of the feedback network drives the amplifier. The total phase shift around a loop is 180° of the amplifier and 180° due to 3-RC section, thus 360°. This satisfies the required condition for positive feedback and circuit works as an oscillator.	
	e)	**Explain the working of astable multi-vibrator using IC 555.**	**4M**
	Ans .	Circuit diagram:   **Explanation:** In the 555 Oscillator circuit above, pin 2 and pin 6 are connected together allowing the circuit to re-trigger itself on each and every cycle allowing it to operate as a free running oscillator.	**Diagram 2M ,** **Explanation 2M, waveform optional**

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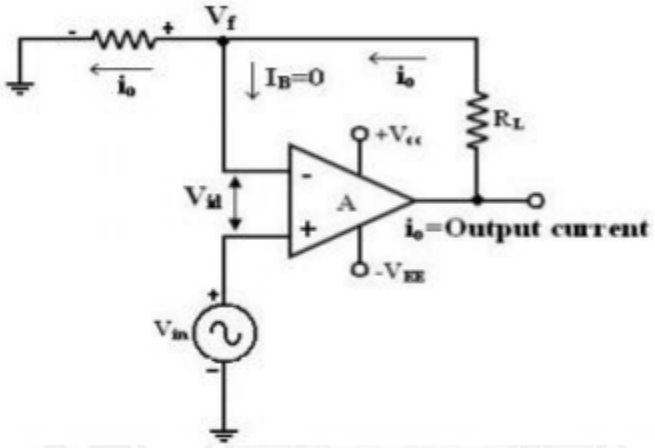
		During each cycle capacitor, C charges up through both timing resistors, R_1 and R_2 but discharges itself only through resistor, R_2 as the other side of R_2 is connected to the *discharge* terminal, pin 7. Then the capacitor charges up to 2/3Vcc (the upper comparator limit) which is determined by the $0.693(R_1+R_2)C$ combination and discharges itself down to 1/3Vcc (the lower comparator limit) determined by the $0.693(R_2*C)$ combination. This results in an output waveform whose voltage level is approximately equal to Vcc – 1.5V and whose output "ON" and "OFF" time periods are determined by the capacitor and resistors combinations. The individual times required to complete one charge and discharge cycle of the output is therefore given as: $$t_1 = 0.693(R_1+R_2)C \ \& \ t_2=0.693(R_2*C)$$ Where, R is in Ω and C in Farads. When connected as an astable multivibrator, the output from the **555 Oscillator** will continue indefinitely charging and discharging between 2/3Vcc and 1/3Vcc until the power supply is removed.	
Q.5		**Attempt any TWO of the following:**	**12M**
	a)	**Draw a circuit diagram of V-I converter of floating load. Derive expression for its output. List any two applications.**	**6M**
	Ans	 **Figure :Voltage to Current converter with floating load**	**2M Diagram** **2M Expression for output** **2M Applications**

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Writing KVL for the input loop,

Voltage $V_{id}=V_f$ and $I_B = 0$, $v_i=R_L i_0$ = where = $i_0=v_i/R_L$

From the figure 2.2.1 input voltage Vin is converted into output current of V_{in}/R_L [V_{in} -> i_0]. In other words, input volt appears across R_1. If R_L is a precision resistor, the output current

($i_0 = V_{in}/R_1$) will be precisely fixed

Applications :
1. Low voltage ac and dc voltmeters
2. Diode match finders
3. LED and Zener diode testers.

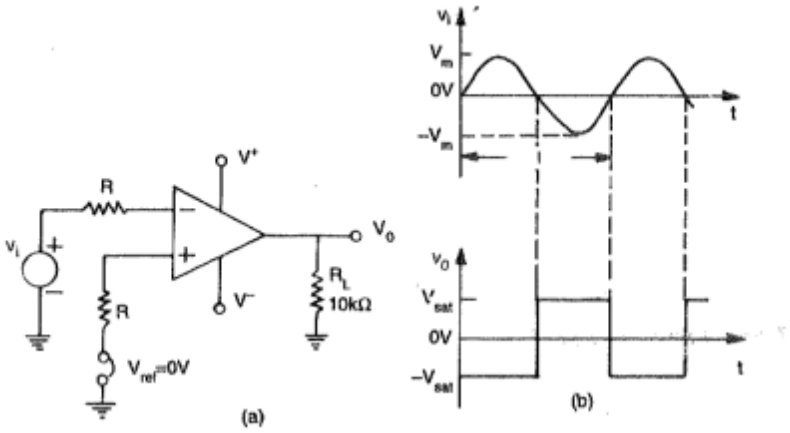
	b)	**Sketch input and output waveform for 2V peak to peak size wave for Inverting ZCD and active Integrator.**	**6M**
	Ans		**3M each for correct input and output waveform**

Fig: (a) ZCD Circuit (b)Input and Output waveforms

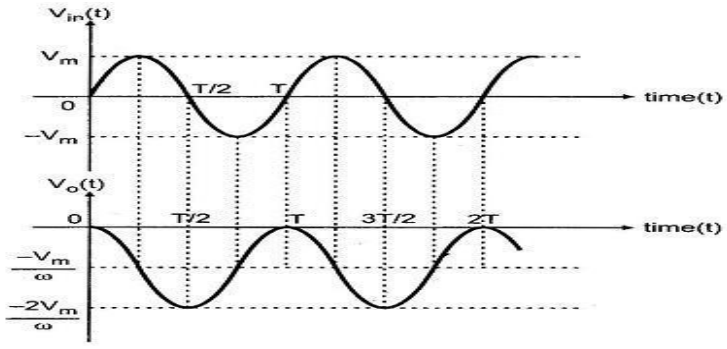


Fig. 2.41 Sine wave input and cosine output

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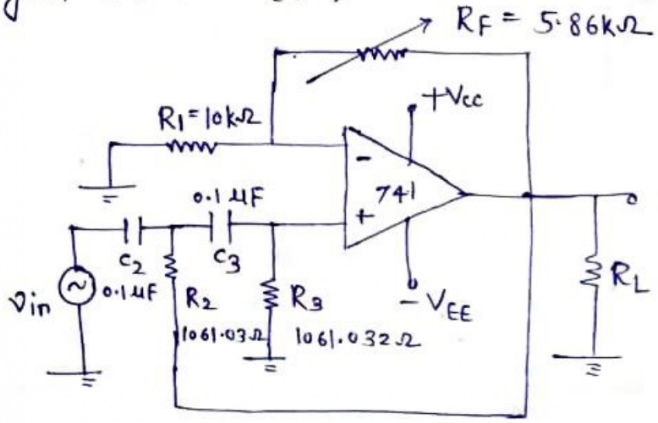
	c)	**Design second order high pass Butterworth filter with higher cutoff frequency of 1.5 kHz. Draw circuit with component values.**	**6M**
	Ans	Given Data :- cut off freq $(f_L) = 1.5$ kHz Sol^n :- Let $R_2 = R_3 = R$ $C_2 = C_3 = C = 0.1\,\mu F$ or (any other value between $0.1\,\mu F$ to $1\,\mu F$) Now $R = \frac{1}{2\pi f_L C} = \frac{1}{2\pi \times 1.5 \times 10^3 \times 0.1 \times 10^{-6}}$ $\therefore R = 1061.032\,\Omega$ since $A_{vf} = 1 + \frac{R_f}{R_1} = 1.586$ $\therefore R_f = 0.586\,R_1$ choose $R_1 = 10\,k\Omega$ $\therefore R_f = 0.586 \times 10 \times 10^3$ $= 5.86\,k\Omega$ Hence the designed circuit Component Values are $C_2 = C_3 = 0.1\,\mu F$ $R_1 = 10\,k\Omega$, $R_F = 5.86\,k\Omega$ $R_2 = R_3 = 1061.032\,\Omega$ Designed circuit :- (4M)  	**1M for calculation of R** **1M for calculation of RF** **4M for Designed circuit with component values**
Q .6		**Attempt Any TWO of the following:**	**12M**
	a)	**Calculate output voltage for open loop non-inverting amplifier. If Vin = 10 mv dc, also draw input and output waveform and draw circuit diagram .**	**6M**

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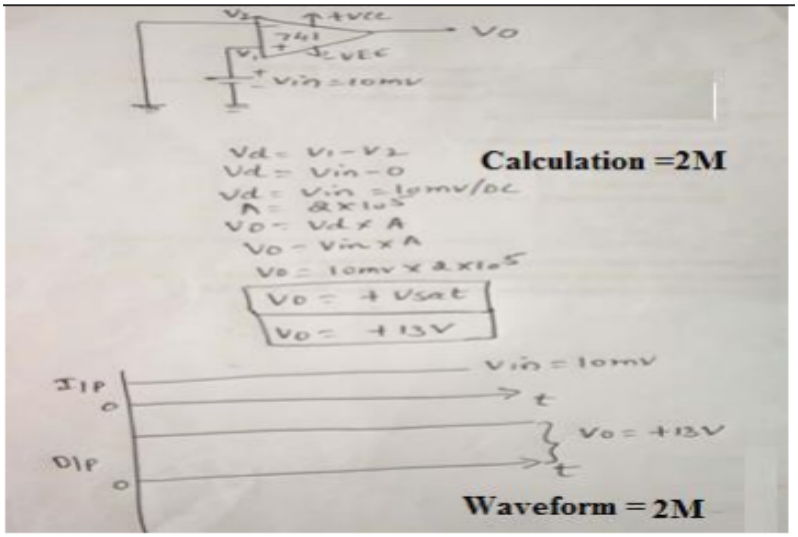
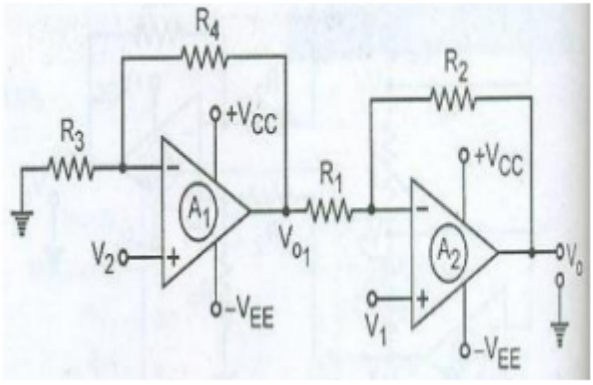
	Ans		**2M for calculation** **2M for input output waveform** **2M for circuit diagram**
	b)	**Explain operation of Instrumentation amplifier with two op-amp with neat diagram.**	**6M**
	Ans	**Two Op-Amp Instrumentation Amplifier:** **Circuit Diagram:** 	**3M Diagram and 3M Explanation**

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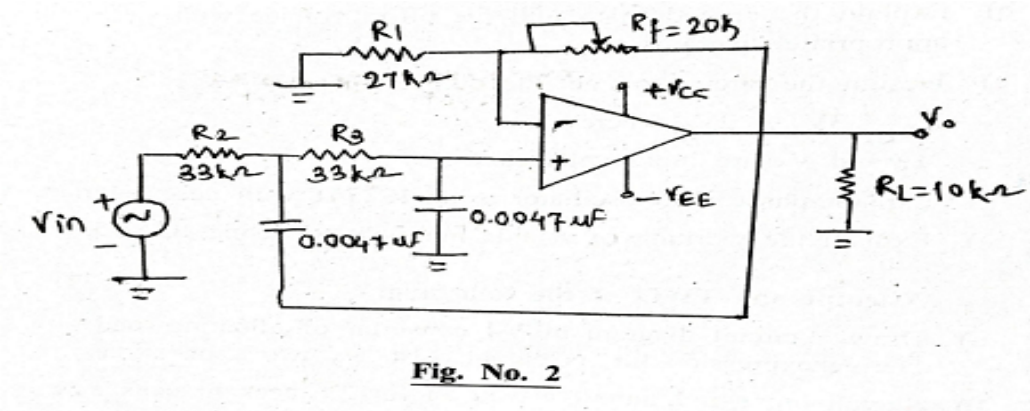
		Derivation: Op amp A_1 is in non-Inverting mode, $\therefore V_{o1} = \left(1+\frac{R_4}{R_3}\right) V_2$ — (1) As Op-amp A_2 is a differential amplifier or subtractor $\therefore V_o = V'_{o1} + V''_{o1}$ $\therefore V'_{o1} = -\frac{R_2}{R_1} \times V_{o1}$ $V''_{o1} = \left(1+\frac{R_2}{R_1}\right) V_1$ $\therefore V_o = -\frac{R_2}{R_1} V_{o1} + \left(1+\frac{R_2}{R_1}\right) V_1$ — (2) Putting equation (1) & (2) we get, $V_o = -\frac{R_2}{R_1}\left(1+\frac{R_4}{R_3}\right) V_2 + \left(1+\frac{R_2}{R_1}\right) V_1$ Assuming, $R_4 = R_1$, $R_3 = R_2$ $\therefore V_o = -\frac{R_2}{R_1}\left(1+\frac{R_1}{R_2}\right) V_2 + \left(1+\frac{R_2}{R_1}\right) V_1$ $\therefore V_o = -\left(1+\frac{R_2}{R_1}\right) V_2 + \left(1+\frac{R_2}{R_1}\right) V_1$ $\therefore \boxed{V_o = \left(1+\frac{R_2}{R_1}\right)(V_1 - V_2)}$ $\boxed{\text{Gain} = A_V = \frac{V_o}{V_1 - V_2} = 1+\frac{R_2}{R_1}}$	
	c)	**From the circuit diagram given in Fig. 2, identify the name of the circuit and calculate cut off frequency and pass band gain**  **Fig. No. 2**	**6M**
	Ans	Given circuit is Second order low pass Butterworth filter	**2M for Identification of circuit** **Calculation of cutoff**

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		cut off freq$_n$ $(f_0) = \frac{1}{2\pi\sqrt{R_2 R_3 C_2 C_3}}$ But since $R_2 = R_3 = R$ and $C_2 = C_3 = C$ we get $f_0 = \frac{1}{2\pi RC}$ $= \frac{1}{2\pi \times 33\times10^3 \times 0.0047\times10^{-6}}$ $= 1026.144$ Hz Pass band voltage gain $K = 1 + \frac{R_F}{R_1}$ $= 1 + \frac{20\times10^3}{27\times10^3}$ $= 1 + \frac{20}{27}$ **= 1.74**	**frequency 2M** **Calculation of Passband gain 2M**