WINTER – 19EXAMINATION

Subject Name: Digital Communication **Model Answer** Subject Code: 17535

Important Instructions to examiners:

1) The answers should be examined by key words and not as word-to-word as given in themodel answer scheme.
2) The model answer and the answer written by candidate may vary but the examiner may tryto assess the understanding level of the candidate.
3) The language errors such as grammatical, spelling errors should not be given moreImportance (Not applicable for subject English and Communication Skills.
4) While assessing figures, examiner may give credit for principal components indicated in thefigure. The figures drawn by candidate and model answer may vary. The examiner may give credit for anyequivalent figure drawn.
5) Credits may be given step wise for numerical problems. In some cases, the assumed constantvalues may vary and there may be some difference in the candidate's answers and model answer.
6) In case of some questions credit may be given by judgement on part of examiner of relevant answer based on candidate's understanding.
7) For programming language papers, credit may be given to any other program based on equivalent concept.

Q. No.	Sub Q. N.	Answer	Marking Scheme
Q.1		**Attempt any THREE of the following:**	**12M**
	(i)	**Compare between analog and digital modulation technique(any four points)**	**4M**
	Ans:	(see table below)	**Any four points 1M each**

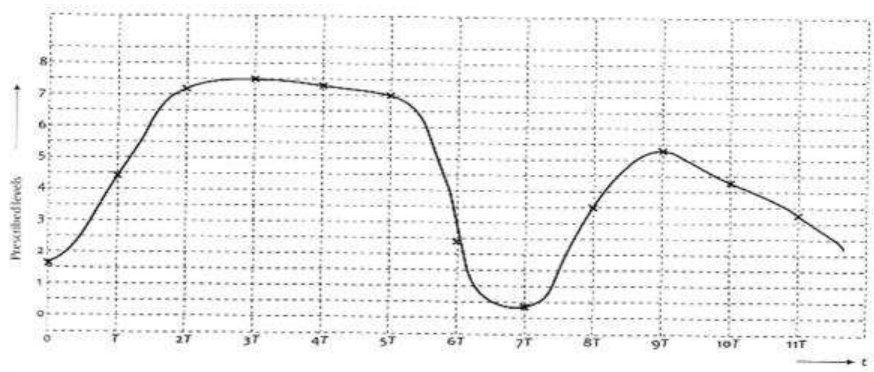
Sr. No	Analog Modulation	Digital Modulation
1	Less bandwidth required	Large bandwidth required
2	More accurate	Less accurate due to quantization error that cannot be avoided or corrected to some extent.
3	Poor noise immunity	High noise immunity as the amplitude of digital signal has two levels only and channel coding (error correcting code) can be used.
4	No signal conditioning and processing are used.	Support complex signal conditioning and processing techniques such as source coding, encryption and equalization.

	(ii)	**Explain Quantization processes with neat W/F.**	**4M**
	Ans:	**QUANTIZATION PROCESS:** • Definition :It is the process of assigning to each one of the sample value of the message signal a discrete value from a prescribed set of a finite number of such discrete values called the 'quantized values'. • Sampling discretizes the continuous time signal only in time but not in amplitude. • The samples obtained by the sampling process can have a continuum of values they are not restricted to any finite set of prescribed values. • The next step in the digitization of an analog signal is the discretization of the amplitudes of these samples obtained through sampling process. • We divide the dynamic range of the analog signal in to a finite number of equal segments and then round off the sample value falling with in a particular segment to the	**Waveform 2M; Expln 2M**

value represented by the ‘ prescribed level’ (Q).

- This process of rounding off is called quantization.

Waveform:



Sample Number	S_0	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}
Actual values of the samples	1.7	4.4	7.2	7.4	7.3	7.0	2.4	0.4	3.4	5.3	4.3	3.2
Rounded off values	2	4	7	7	7	7	2	0	3	5	4	3
Binary code for rounded value	010	100	111	111	111	111	010	000	011	101	100	011

(iii) Define: **4M**

(1) **Code word**
(2) **Code Rate**
(3) **Hamming weight**
(4) **Code efficiency**

Ans: **1M each**

Code word:-
In block code, each block of ‘k’ information bit is encoded into a block of ‘n’ bits(n>k). this n-bit block is called code word.

Code rate:-
The ratio of message bits (k) and the encoder output bits(n) is called code rate. It is defined by ‘r’. mathematically expressed as $r = k / n$; $0 < r < 1$

Hamming weight:-
The number of non-zero symbols in a symbol sequence or **Hamming weight** is the number of "1" bits in the binary sequence.

Code efficiency:-
Code efficiency in Huffman coding is the ratio of entropy of the source to the average length of the code word.

(iv) Describe FDM techniques with block diagram of YX and RX. **4M**

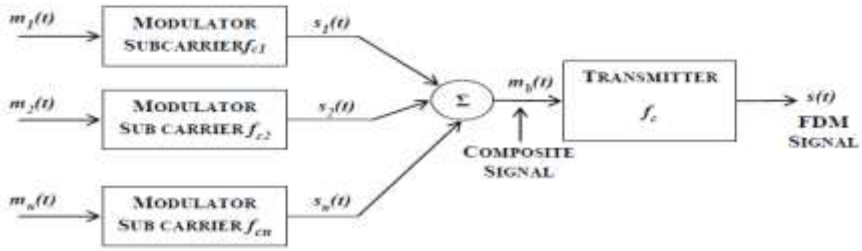
Ans: **2M TX diag with expl RX diag,with expln 2M**

FREQUENCY DIVISION MULTIPLEXING (FDM):

- FDM is an analog multiplexing technique in which many signals are sent simultaneously at the same time but are separated from each other in the frequency domain.

FDM TRANSMITTER:

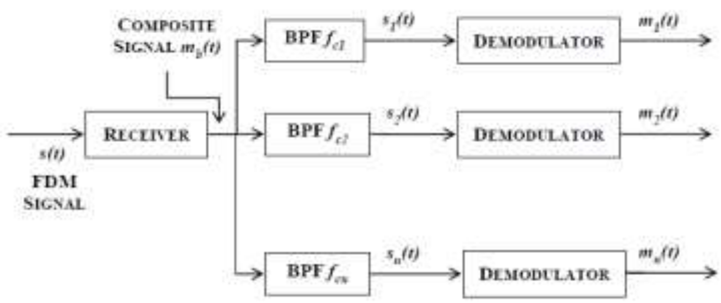
- In FDM, the transmission channel is shared by multiple signals, each being allotted a portion of the spectrum of the bandwidth. A generalized block diagram of FDM transmitter is shown below



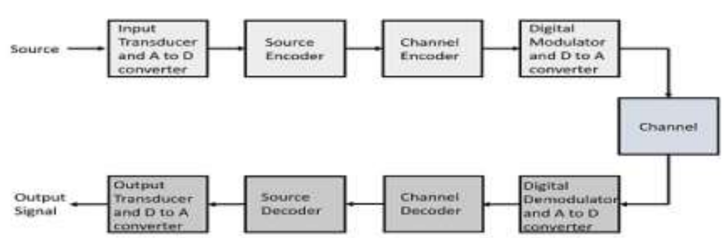
- A number of analog signals (or digital signals converted into analog) *mi(t)*, *i* = 1, 2, . . ., *n* are multiplexed onto the same transmission medium. Each signal *mi(t)* is modulated onto a carrier *fci*.
- As multiple carriers are to be used, each is referred to as a *subcarrier*. Any type of analog modulation may be used. The resulting analog signals are summed together to produce a composite signal, *mb(t)*.
- The composite signal may be shifted, as a whole, to another carrier frequency by an additional modulation step
- This second modulation step need not use the same modulation technique as the first. Thus, the FDM signal generated may be transmitted over a suitable medium.

FDM RECEIVER:

- The FDM receiver is shown in Figure 5.5. The FDM signal is received by the receiver and demodulated to retrieve the composite signal *mb(t)* which is further amplified.
- This composite signal is passed through *n*band pass filters, each filter having a center frequency equal to the subcarrier frequency *fci*.
- In this way the composite signal is split into its component signals. Each component signal is further demodulated to obtain the analog outputs that were originally transmitted. If required, these signals are stored and displayed.

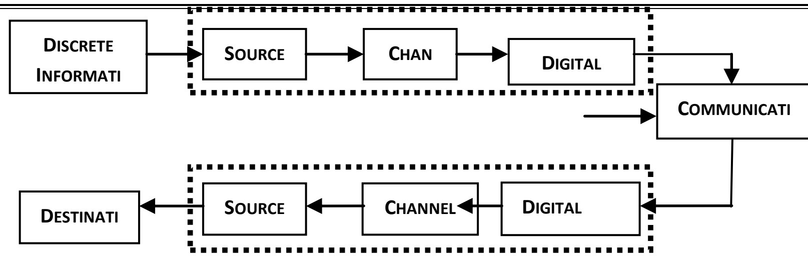


b)	Attempt any ONE of the following:	6M
(i)	**Draw the block diagram of basic digital communication system and explain each block.State any two advantages and disadvantages of system.**	**6M**
Ans:	**Block diagram of a digital communication system**	**Diag. 2M Expln 2M Any 2 adv. & 2 disadv 2M**



Basic Elements of a Digital Communication System

(½ M each)



<u>DISCRETE INFORMATION SOURCE:</u>

- The information to be transmitted originates here. These information/messages may be available in digital form, as for instance, in the case of the output of a teletype system, or it may be available in an analog form.
- If it is analog it is sampled and digitized using an A/D converter to make the final source output to be digital in form.

<u>SOURCE ENCODER :</u>

- Generally, the bit stream at the source output will have considerable redundancy and so will not be efficient representation of the message or information given by the source, from the point of view of the number of digits used.
- A fewer number of digits might be sufficient to convey the information. The source encoder therefore reduces the redundancy by performing a one to one mapping of its input bit stream in to another bit stream at its output, but with fewer digits.
- Thus in a way it performs data compression.

<u>CHANNEL ENCODER:</u>

- The channel encoder is intended to introduce controlled redundancy into the bit stream at its input in order to provide some amount of error- correction capability to the data being transmitted.
- The data gets corrupted by the additive noise on the channel and this gives rise to the possibility of the channel decoder committing mistakes in the decoding of the data received from the channel.
- Redundancy helps in detecting erroneously decoded bits and makes it possible to correct the errors before passing on the data to the source decoder.

<u>DIGITAL MODULATOR:</u>

- The physical channels are basically analog in nature; the digital modulator takes each digital binary digit at its input and maps it, in a one –to – one fashion, into a continuous waveform.
- Binary 'zero' at its input is mapped into a continuous signal $s_o(t)$ and binary 'one' is mapped into another continuous signal $s_1(t)$.
- This is called binary modulation.

<u>PHYSICAL CHANNEL:</u>

- The digitally modulated signal is passed on to the physical channel, which is nothing but the physical medium through which the signals are transmitted.
- It may take a variety of forms- a pair of twisted wires, coaxial cable, a wave guide, a microwave radio, or an optical fiber.
- A long distance telephone call for instance may go through each one of these different forms of physical channels at different stages of its passage from the place of origin to the final destination.
- During its passage through the channel, the signal gets corrupted by noise. This

noise may be thermal noise originating from electronic circuits or atmospheric noise, or manmade noise, or as is generally the case, a combination of most or all of them.

THE DIGITAL DEMODULATOR:

- The digital demodulator of the receiver receives the noise corrupted sequence of waveforms from the channel and by inverse mapping tries to give at its output, an estimate of the sequence of the binary digits that were available at the input of the digital modulator at the transmitting end.

THE CHANNEL DECODER:

- The output sequences of digits from the digital demodulator are fed to the channel decoder. Using its knowledge of the type of coding performed by the channel encoder at the transmitting end and using the redundancy introduced by the channel encoder, it produces as its output, the output of the source coder of the transmitter with as few errors as possible.

THE SOURCE DECODER:

- Using its knowledge of the type of encoding performed by the source encoder of the transmitter, the source decoder of the receiver tries to reproduce at its output, a replica of the output of the digital source at the transmitting end.
- It may not be an exact replica of the source output. There may be some errors in the sense that some of the binary 1's produced by the source might be received by the user at the destination as 0's and vice versa.
- In a long sequence of binary digits transmitted, the fractional number of times such errors occur on the average is referred to as the 'probability of error'. A typical value of the probability of error may be say 1 in a hundred million, i.e., 10^{-8}.

Advantages of Digital Communication : (any 2)

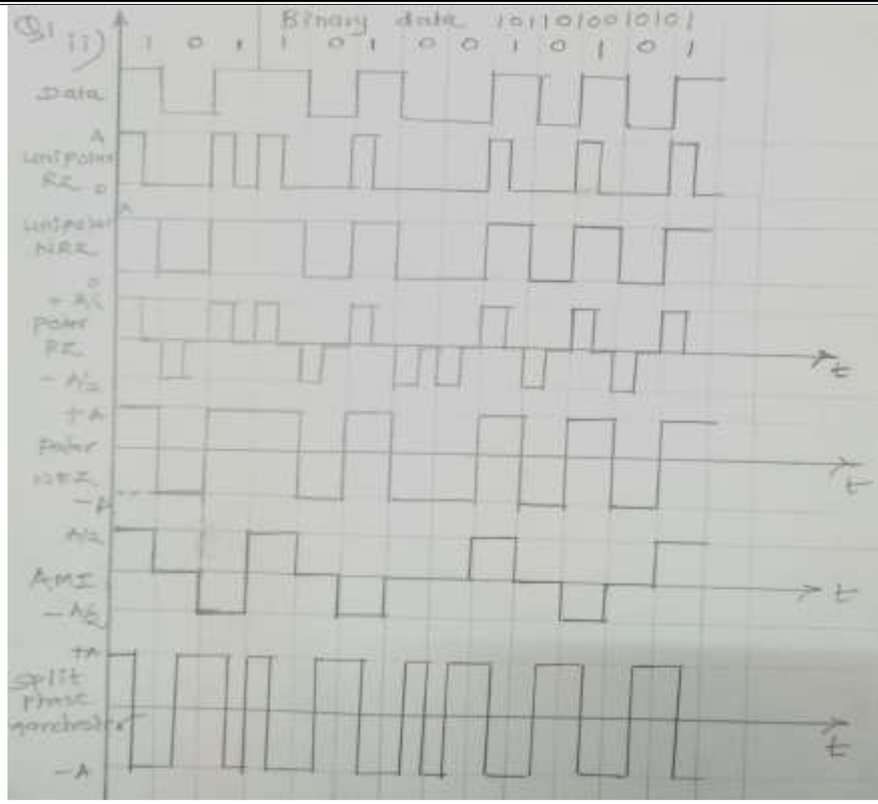
1. High noise interference tolerance due to digital nature of the signal.
2. With channel coding, error detection and correction at receiver is possible.
3. It provides us added security to our information signal i.e. Data encryption is possible for greater security.
4. Cheaper due to advances in digital VLSI technology.
5. Digital information can be saved and retrieved when necessary.
6. Large data storage is possible.

Disadvantages of Digital Communication : (any 2)

1. Large System Bandwidth: - Digital transmission requires a large system bandwidth to communicate the same information in a digital format as compared to analog format.
2. High power consumption (Due to various stages of conversion).
3. Needs synchronization
4.Sampling Error.

	(ii)	**Encode the following Binary data stream into unipolar RZ,unipolar NRZ,polar RZ,polar NRZ,AMI and split phase manchestar code.Data stream is 1011010010101**	**6M**

Ans: **1M each**

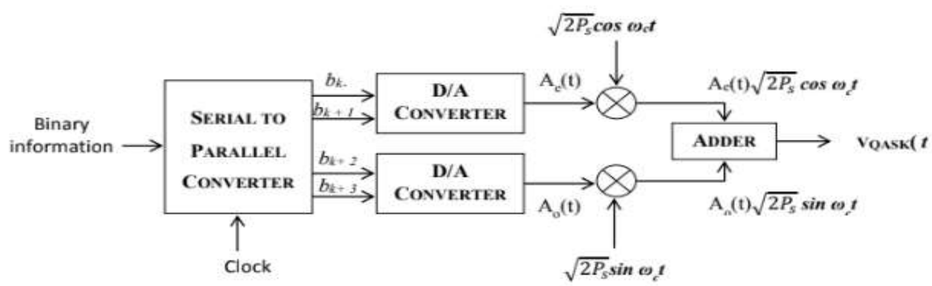


Q.2 **Attempt any TWO of the following:** **16M**

a) **Draw block diagram of 4 QAM and 8 QAM and explain its and also draw the phasor diagram of 8 QAM and 16 QAM.** **8M**

Ans: **(Note: 2M each for Transmitter diagram and explanation 2M ; phasor diagram 1M each)**

Basic block diagram of QAM transmitter:



Explanation:-

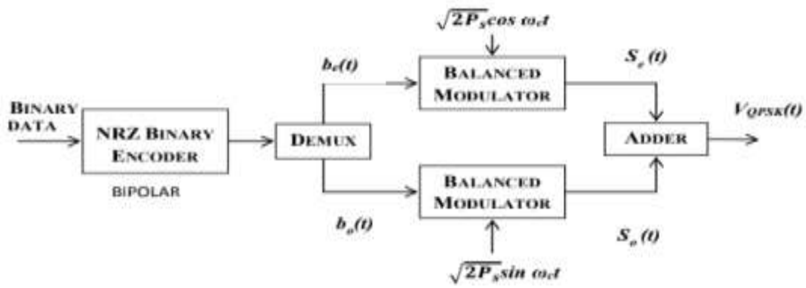
- The bit stream b(t) is applied to the serial to parallel converter, operating on a clock which has a period of Ts, which is the symbol duration. The bits b(t) are stored by the converter and then presented in the parallel form. The four bit symbols are bk + 3, bk+ 2, bk + 1, bk.
- Out of these four bits, the first two bits are applied to a D/A converter and the other two bits are applied to the second D/A converter.
- The output of the first converter is Ae(t), which is modulated by the carrier √2Ps cosωct whereas the output of the second D/A converter, Ao(t) is modulated by the carrier √2Pssinωct in the balanced modulators.

- Ae(t),Ao(t)arevoltage levels generated by the convertor -3,-1,+1,+3 volts.
- The balanced modulator outputs are added together to get the QASK output signal which is expressed as,

$V_{QASK/\ QAM}(t) = Ae(t)\sqrt{2Ps}\cos\omega ct + Ao(t)\ \sqrt{2Ps}\sin\omega ct$

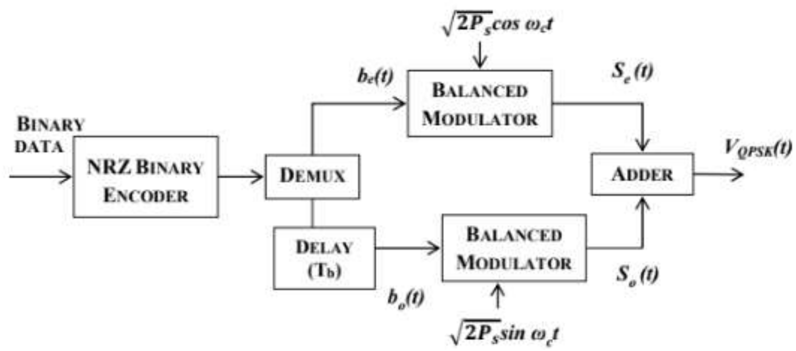
Block diagram of 4 QAM transmitter:-

<u>NOTE:- 4 QAM is equivalent to QPSK</u>



QPSK Transmitter (non - offset)

OR



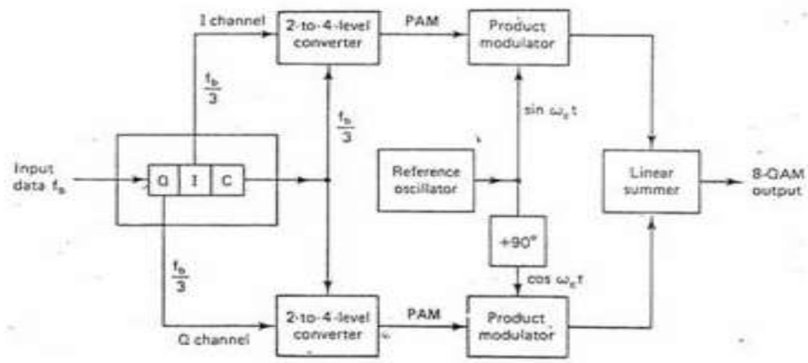
QPSK Transmitter (offset)

Explanation:-

- The input data sequence is first converted into a bipolar NRZ signal b(t). The value of b(t) =
  + 1 for logic 1 input and b(t) = - 1 when the binary input is equal to 0.
- The De-multiplexer (DEMUX) will divide b(t) into two separate bit streams bo(t) and be(t).
- The bit stream be(t) consists of only the even numbered bits 2, 4, 6, 8, ... whereas bo(t) bitstream consists of only the odd numbered bits i.e., 1, 3, 5, ... as shown in above Figure.
- Each bit in the even and odd stream will be held for a period of 2Tb. This duration is called assymbol duration Ts. Thus, every symbol contains two bits.
- The bit stream be(t) is superimposed on a carrier √2Pscosωct and the bit stream bo(t) is superimposed on a carrier √2Pssinωct by using two balanced modulators (or multipliers) to generate se(t) and so(t). These two signals are basically BPSK signals.
- These signals are then added to generate the QPSK output signal VQPSK(t) given by,

$$\mathbf{V_{QPSK}(t) = bo(t)\ \sqrt{2Ps}\sin\omega ct + be(t)\sqrt{2Ps}\cos\omega ct}$$

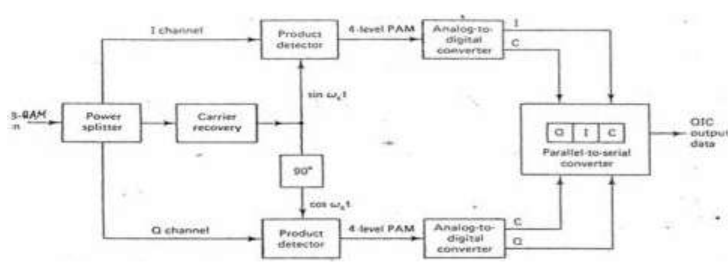
Block diagram of 8 QAM transmitter :-



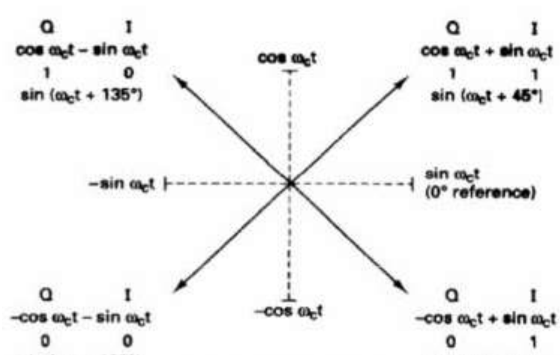
Explanation of 8 QAM transmitter:-

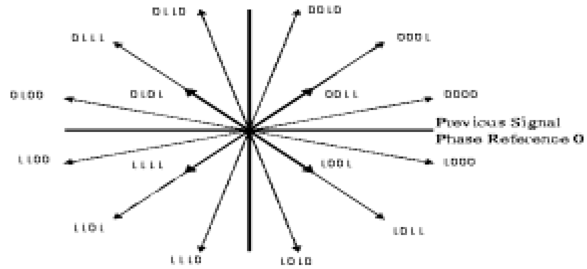
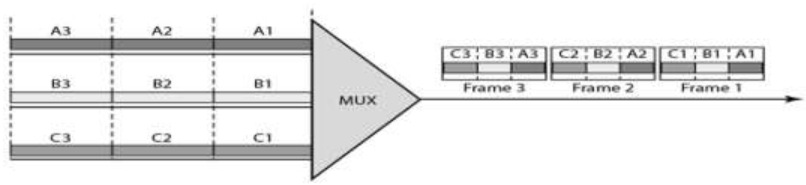
- Figure shows the block diagram of an 8-QAM transmitter only difference between the 8-QAM transmitter and the 8-PSK transmitter shown in figure is the omission of the inverter between the C channel and the Q product modulator.
- As with 8-PSK, the incoming data are divided into groups of three bits (tri bits): the I, Q and C bit streams, each with a bit rate equal to one-third of the incoming data rate.
- The 'I' and 'Q' bits determine the polarity of the PAM signal at the output of the 2-to-4-level converters, and the C channel determine the magnitude.
- Because the C bit is fed uninverted to both the 'I' and the 'Q' channel 2-to-4-level converters, the magnitude of the 'I' and 'Q' PAM signals are always equal. Their polarities depend on the logic condition of the 'I' and 'Q' bits and therefore may be different the truth table for the 'I 'and 'Q' channel 2-to-4-level converters; they are identical.

Block diagram of 8 QAM receiver:-



Phasor diagram of 8-QAM:-



		Phasor diagram of 16-QAM:-  	
	b)	**Describe synchronous Time Division Multiplexing with neat diagram. State any two advantages, disadvantages and applications of TDM**	**8M**
	Ans:	**SYNCHRONOUS TDM:**  **Explanation:** • In synchronous TDM the term synchronous means that the multiplexer allocates exactly the same time slot to each device at all times whether or not a device has anything to transmit. • For example, time slot 1 is assigned to device 1 alone and cannot be used by any other device. Each time its allocated time slot comes up, a device has the opportunity to send a portion of its data. If a device is unable to transmit or does not have data to send, its time slot remains empty. • Time slots are grouped into frames. In a system with "n" input lines (devices), each frame has at least "n" time slots, with each slot allocated to carrying data from a specific device. Thus, the time slots dedicated to a given device occupy the same location in each frame and constitute that device's channel. **ADVANTAGES(Any two)** 1. Full channel bandwidth is available to each sending device. 2. Intermediation distortion is absent. 3. TDM circuitry is not very complex. 4. The problem of crosstalk is not very serious. **DISADVANTAGES (Any two)** 1. Synchronization is essential between sending and receiving end. 2. Complex to implement **APPLICATIONS (Any two)** 1. ISDN telephone lines and wire line telephone system 2. Radio broadcasting 3. Telemetry 4. Data processing	**Diagram 3M** **2M** **1M(½ each)** **1M(½ each)** **1M(½ each)**
	c)	**Explain generation and detection procedure of VRC and CRC with neat diagram and give one example of each.**	**8M**

	Ans:	VERTICAL REDUNDANCY CHECKING (VRC):	4M

Ans: **VERTICAL REDUNDANCY CHECKING (VRC):** **4M**

- Vertical Redundancy Checking (VRC) is the simplest error detection scheme and is generally referred to as Character parity or simply Parity.
- With character parity, each character has its own error detection bit called the parity bit. Since the parity bit is not actually a part of the character, it is considered as a redundant bit.
- An n- character message would have n redundant parity bits. Therefore, the number of error detection bits is directly proportional to the length of the message.
- Parity can be of two types:

1. Odd parity
2. Even parity

In odd parity, the total number of 1's in the entire message should be odd whereas in even parity, the total number of 1's in the message should be even.

- With character parity (VRC), a single parity bit is added to each character to force the total number of logic 1's in the character, including the parity bit, to be either an odd number (odd parity) or an even number (even parity).
- For example, the ASCII code for the letter C is 43H or P1000011, where the P bit is the parity bit. There are three logic 1's in this code, not counting the parity bit.
- If odd parity is used, the P bit is made logic 0, keeping the total number of logic 1's at three, This is an odd number.
- If even parity is used, the P bit is made logic 1, making the total number of logic 1's four, which is an even number.
- The main advantage of parity is its simplicity.

Example: Determine the VRC for the following ASCII encoded message: THE CAT. Use odd parity for the VRC **4M**

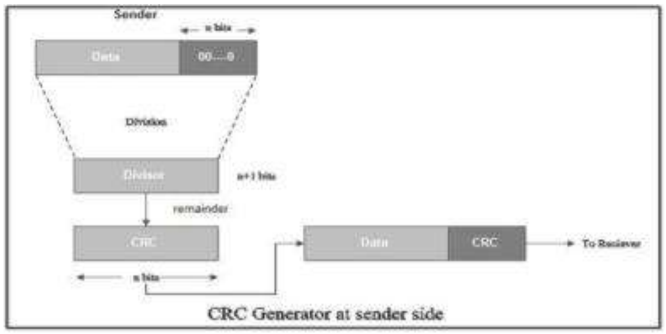
Solution:

Character	Bit position	T	H	E	space	C	A	T
ASCII Code	B_1	0	0	1	0	1	1	0
	B_2	0	0	0	0	1	0	0
	B_3	1	0	1	0	0	0	1
	B_4	0	1	0	0	0	0	0
	B_5	1	0	0	0	0	0	1
	B_6	0	0	0	1	0	0	0
	B_7	1	1	1	0	1	1	1
Parity Bit (VRC)	B_8	0	1	0	0	0	1	0

The various steps followed in the CRC method are

1. A string of n as is appended to the data unit. The length of predetermined divisor is n+ 1.

2. The newly formed data unit *i.e.* original data + string of n as are divided by the divisor using binary division and remainder is obtained. This remainder is called CRC.

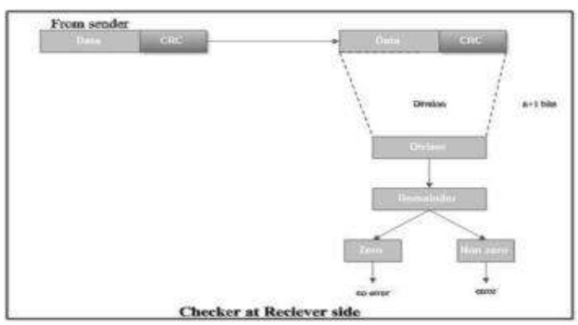


CRC Generator at sender side

3. Now, string of n 0's appended to data unit is replaced by the CRC remainder (which is also of n bit).
4. The data unit + CRC is then transmitted to receiver.
5. The receiver on receiving it divides data unit + CRC by the same divisor & checks the remainder.
6. If the remainder of division is zero, receiver assumes that there is no error in data and it accepts it.
7. If remainder is non-zero then there is an error in data and receiver rejects it.

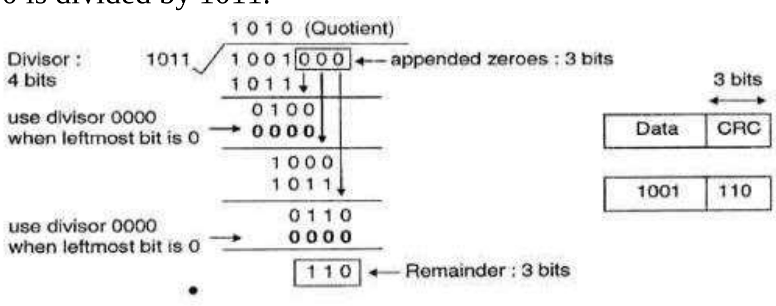
• For example, if data to be transmitted is 1001 and predetermined divisor is 1011. The procedure given below is used:

1. String of 3 zeroes is appended to 1011 as divisor is of 4 bits. Now newly formed data is 1011000.



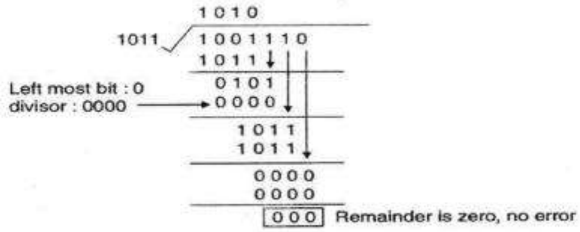
Checker at Reciever side

1. Data unit 1011000 is divided by 1011.



CRC generated (Binary division)

2. During this process of division, whenever the leftmost bit of dividend or remainder is 0, we use a string of 0's of same length as divisor. Thus in this case divisor 1011 is replaced by 0000.
3. At the receiver side, data received is 1001110.
4. This data is again divided by a divisor 1011.
5. The remainder obtained is 000; it means there is no error.



CRC decoded (binary division)

• CRC can detect all the burst errors that affect an odd number of bits.
• The probability of error detection and the types of detectable errors depends on the choice of divisor.
• Thus two major requirement of CRC are:
(a) CRC should have exactly one bit less than divisor.
(b) Appending the CRC to the end of the data unit should result in the bit sequence which is exactly divisible by the divisor.

Q.3		**Attempt any FOUR of the following :**	**16M**
	a)	**Explain slope overload error and granular noise in delta modulation with neat diagram. Describe how it can be reduced.**	**4M**

Ans: **SLOPE-OVERLOAD DISTORTION:**

1.5 M FOR EACH NOISE

• If the slope of the analog signal x(t) is much higher (steep) than that of the approximated signal xq(t) over a long duration then xq(t) will not follow x(t) at all as shown in Figure
• The difference between x(t) and xq(t) is called the slope-overload distortion or the slope-overload error. Thus, slope-overload error occurs when the slope of x(t) is much higher than xq(t).

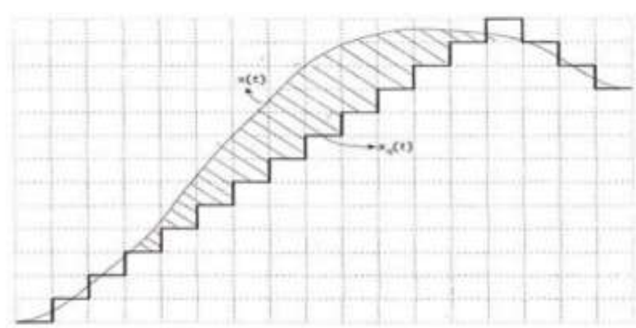


Fig. Illustrating the phenomenon of slope overload in linear delta modulation

GRANULAR NOISE:
• When the input signal x(t) is relatively constant in amplitude, the approximated signal xq(t) will hunt above and below x(t) as shown in Figure. This leads to a noise called granular noise.
• It increases with increase in step size δ. To reduce granular noise, the step size should be as small as possible. However, this will increase slope-overload distortion.

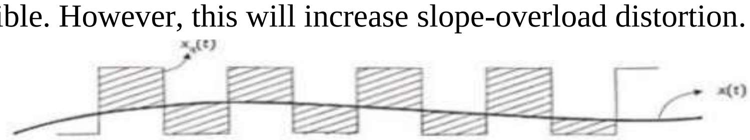
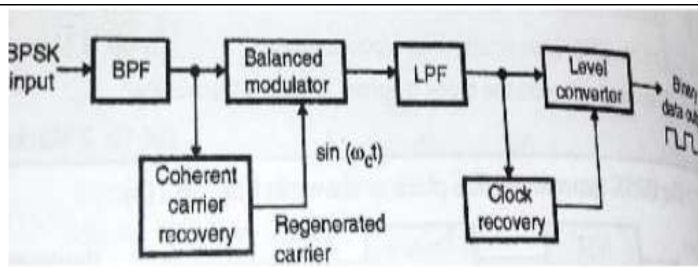


Fig. Granular noise

½ M FOR

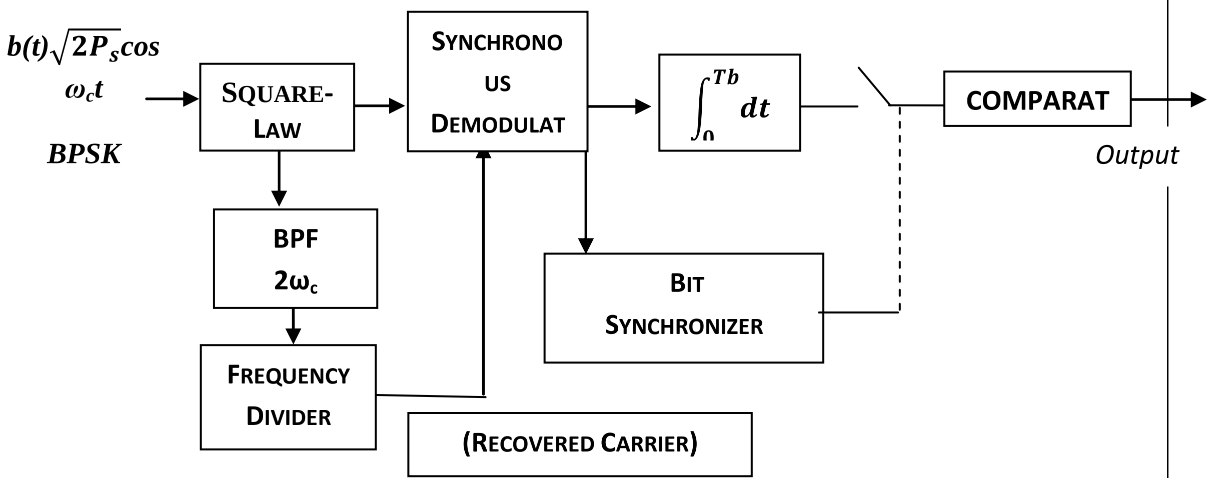
		REDUCTION OF NOISE The slope overload error can be reduced by increasing slope of the approximated signal xq(t). If slope of xq(t) can be increased and hence the slope overload error can be reduced by either increasing the step size δ or by increasing sampling frequency fs. Granular noise can be reduced by keeping the step size δ should be as small as possible.	**Each reduct--on of noise**
	b)	**List types of errors and their causes.**	**4M**
	Ans:	**Types of error**: 1. Single bit error: Single-bit error occurs when only one bit of a given data string is in error (changed from 0 to 1 or from 1 to 0). 2. Burst error: A burst error or multiple-bit error occurs when two or more bits within a given data string is in error. **Causes of errors:** Due to addition of noise in transmission & reception of data following errors occur. 1. If data block is lost in the network as it has been delivered to wrong destination. 2. If two or more bits from data unit such as a byte change from 1 to 0 or 0 to 1.	**Types of error 2M** **Causes of errors 2M**
	c)	**Draw and explain PSK receiver.**	**4M**
	Ans:	 **Block diagram of PSK receiver** **Working of PSK receiver** i) The coherent carrier recovery circuit detects and regenerates a carrier signal sin ωct. This regenerated carrier has the same frequency and phase as the carrier used at the transmitter. ii) So the regenerated carrier is known as coherent carrier. iii) The filtered BPSK signal along with the regenerated carrier is applied to a balanced modulator which acts as a product detector. $\therefore$ B.M. output $=$ BPSK $\times$ Regenerated carrier $= (\pm \sin \omega_c t \times \sin \omega_c t = \pm \sin^2 \omega_c t)$ But $\sin^2 \theta = \frac{1}{2} - \frac{1}{2} \cos 2\theta$ $\therefore$ B. M. output $= \pm \frac{1}{2} \mp \frac{1}{2} \cos 2 \omega_c t$ iv) The BM output consists of a dc term and a term having frequency twice the carrier frequency. v) The BM output is passed through LPF which allows only the second term to pass through. $\therefore$ LPF output $= \mp \frac{1}{2} \cos 2 \omega_c t$ vi) The LPF is applied to the level detector and clock recovery circuit at the output of level detector we get the following output.	**Block diagra2 M** **2M expl**

$$-\frac{1}{2}\cos\omega_c t \rightarrow \frac{1}{2}V\text{ (logic 1)}$$

$$+\frac{1}{2}\cos\omega_c t \rightarrow -\frac{1}{2}V\text{ (logic 0)}$$

vii) Thus the binary signal is obtained at the output.

OR



- The received BPSK signal at the receiver input is in the form:

$$V_{BPSK}(t) = b(t)\sqrt{2P_S}\cos\omega_c t$$

- The demodulation technique used is coherent demodulation. The synchronous detection technique requires a locally generated synchronized carrier signal $\cos\omega_c t$.
- This carrier is recovered from the received BPSK signal. The carrier recovery is done as follows:
- The received signal is passed through a square law device and we get a squared signal at the output of the square law device.
- Output of the square law device=$(\pm 1)^2 2P_S\cos^2\omega_c t = 2P_S\cos^2\omega_c t$

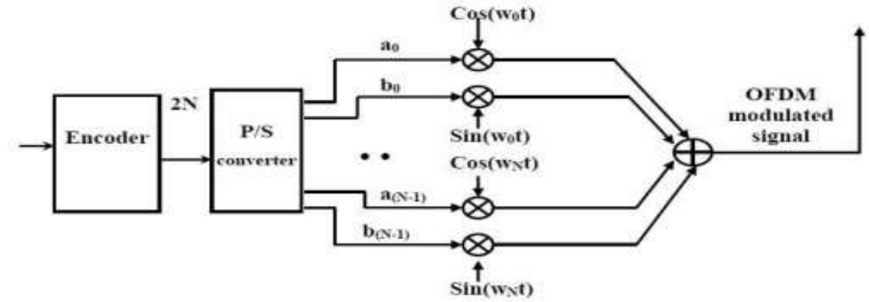
But, $$\cos^2\omega_c t = ½\,[\,1 + \cos 2\,(\omega_c t\,)\,]$$

- The RHS of this expression shows that the output of the square law device consists of a dc term [1/2] and the 2nd harmonic of the carrier [1/2 cos2(ω_ct)].
- Only the 2nd harmonic component is allowed to pass through the BPF, the center frequency of which is adjusted to $2\omega_c$. Thus, the output of the BPF is cos2(ω_ct) neglecting the amplitude. The dc component is blocked by the filter.
- The BPF output is then passed through a frequency divider to recover the carrier signal cos(ω_ct). Thus, the carrier is recovered from the received BPSK signal.
- The received BPSK signal at the input of receiver and the recovered carrier signal are multiplied by the synchronous modulator which is nothing but a multiplier.

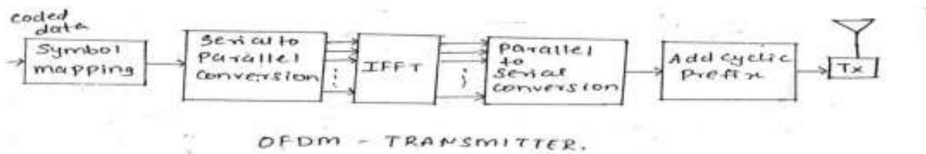
$$\text{Output of the multiplier} = b(t)\sqrt{2P_s}\cos(\omega_c t) \times \cos(\omega_c t)$$

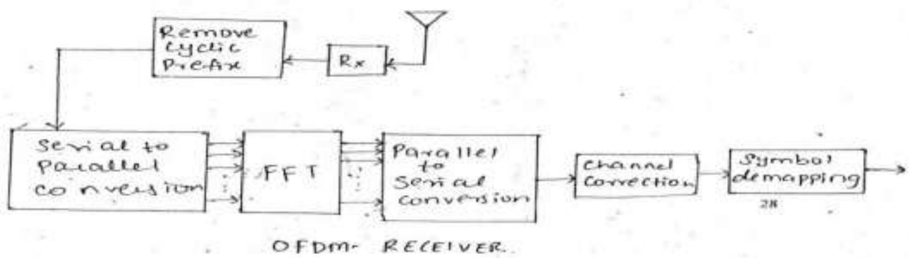
$$= b(t)\sqrt{2P_s}\cos^2(\omega_c t)$$

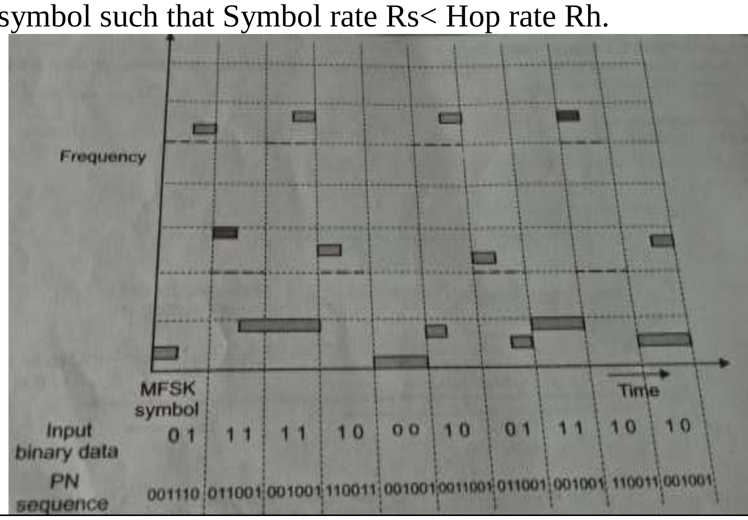
		$= b(t)\sqrt{2P_s}\,[\,½ + ½\cos 2(\omega_c t)\,]$ • This signal is applied to an integrator. The bit synchronizer device is able to recognize precisely the moment which corresponds to the end of the time interval allocated to one bit and the beginning of the next. The bit synchronizer closes the switch S_1momentarily to discharge (dump) the integrator capacitor at the beginning of every bit interval and leaves the switch S_1 open for the entire bit duration so that the integrator can produce an output proportional to its input voltage. The switch S_1 is closed again very briefly at the end of the bit interval. Thus, this circuit is called an "integrate-and-dump" circuit. • The output of the integrator is the output of the BPSK receiver. This output signal is made available by closing the switch S_2at the end of each bit interval but immediately before the closing of switch S_1. The switch S_2 is called the sampling switch and is operated by the bit synchronizer. The output of the integrator is given by, $v_o(kT_b) = b(t)\sqrt{2P_s}\int ½\,dt + b(t)\sqrt{2P_s}\int ½\cos 2(\omega_c t)\,dt$ $= b(t)\sqrt{2P_s}\,(T_b/2)$ $=(\pm 1)\sqrt{2P_s}\,(T_b/2)$ • Since the integral of sinusoid over a whole number of cycles has the value zero. In the above equation, $T_b$is the bit interval of each bit. Thus, we see that the demodulator output is the transmitted bit stream b(t).	
	d)	**With the help of OFDM block diagram, explain its working.**	**4M**
	Ans:	Figure below shows the conceptual diagram highlighting the orthogonal (OFDM) multiple carrier modulation scheme. The ai – s in the diagram indicates the modulating signal in the I – path and the bi – s are the modulating signals in the Q – path. The 'encoder' in a practical system performs several operations but if of no special significance at the moment. All the cosine modulated signals are added algebraically and similarly are the sine modulated signals. The overall I – phase and Q – phase signals together form a complex baseband OFDM signal. At this point, one may interpret the scheme consisting of a bank of N parallel QPSK modulators driven by N orthogonal sub carriers.	**Block diagram** **And working :** **2M each**



OR





	e)	**Explain fast frequency hopping with suitable diagram.**	**4M**
	Ans:	Fast frequency hopping-In fast frequency hopping, multiple frequencies or hops are used to transmit one symbol. That is each symbol, several hops takes place. So several frequencies changes for one symbol such that Symbol rate Rs< Hop rate Rh. 	**1M** **Diagram 3M**

Q.4	**a)**	**Attempt any THREE of the following:**	**12M**
	(i)	**State sampling theorem and write about its importance.**	**4M**
	Ans:	Statement.: Sampling theorem states that a band-limited signal of finite energy having the highest frequency component fmHz can be represented and recovered completely from a set of samples taken at a rate of fs samples per second provided that fs ≥ 2fm. Importance: If the sampling rate fs< 2fx (Under Sampling), then the sidebands of the signal overlap and x(t) cannot be recovered without distortion from Xs(f). This distortion is referred to as Aliasing or Fold-over distortion.	**Statement& Importance 2M each**

(ii) With example explain how hamming code is used for single bit error connection implications. **4M**

Ans: Hamming codes are basically linear block codes. It is an error correcting code. The parity bits are inserted in between the data bits as shown below.

D7	D6	D5	P4	D3	P2	P1	
7bit	6bit	5bit	4bit	3bit	2bit	1bit	7-bit hamming code

Where D-data bits and P- parity bits. The hamming coded data is then transmitter. At the receiver it is coded to get the data back. The bits (1, 3, 5, 7), (2, 3, 6, 7) and (4, 5, 6, 7) are checked for even parity or odd parity, if all the 4-bit groups mentioned above possess the even parity (or odd parity) then the received code word is correct but if the parity is not matching then error exist. Such error can be located by forming a three bit number out of three parity checks. This process can be well explained by following example,

For example: Suppose a 7-bit hamming code is received as 1110101 (for transmitter data 1111) and parity used is assumed to be even .hence we can detect and correct the code as

Step1: Received 7bit hamming code is applied to hamming code format as

D7	D6	D5	P4	D3	P2	P1
1	1	1	0	1	0	1

Step2: Check bits for P4 bit

i.e. P4	D5	D6	D7	
0	1	1	1	odd parity hence error

So, P4=1

Step 3: check bits for P2bit

i.e. P2	D3	D6	D7	
0	1	1	1	odd parity hence error

So, P2=1

Step 4: check bits for P1 bit

i.e. P1	D3	D5	D7	
1	1	1	1	even parity hence no error

So, P1= 0 Hence the error word is E = 1 1 0

Step 5: decimal equivalent of 110 is 6 hence 6thbit is incorrect so invert it and the correct code word will be,

D7	D6	D5	P4	D3	P2	P1
1	0	1	0	1	0	1

Hence the single bit error can be corrected using hamming code.

Hamming Code Explana- -tion 2M

Example with Steps 2M

(iii) Draw block diagram of SDM multiplexing and explain each block. **4M**

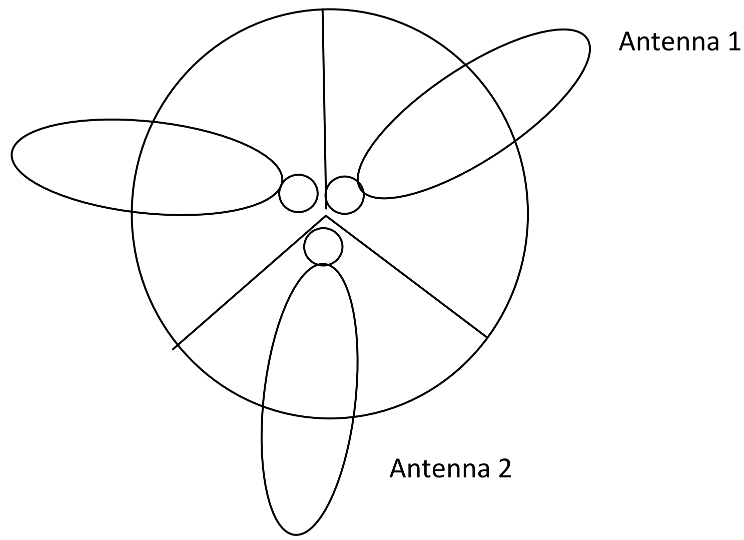
Ans: **SDM** is space division multiplexing. Figure shows block diagram of SDM .When we want to transmit multiple message with maximum reuse of the given resources like time and frequency.it can be done by grouping many separate wires in to a common cable enclosure. SDM system does not require any multiplexing equipment.

It is usually combined with other multiplexing techniques to be better utilizing the physical channels.

Block diagram And working : 2M

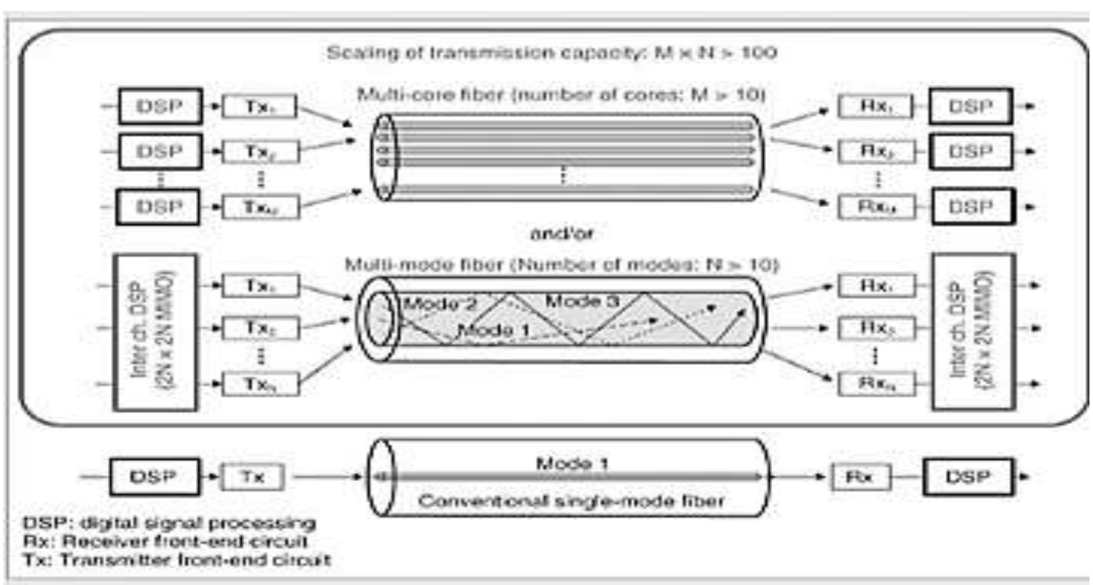
1. In SDM signal can be transmitted by different directional antennas or the signals received by the multidimensional antenna can be combined to get all of them back.
2. Three directional antennas can be transmitted simultaneously. Space division multiplexing is just like a high way with the provision of different lines.

each



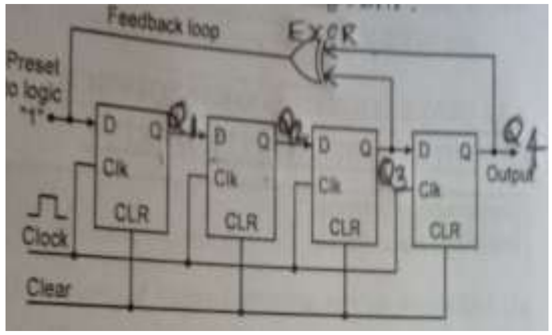
Block diagram of space division multiplexing

OR



	(iv)	**Explain 4 bit PN sequence generator used in spread spectrum techniques.**	**4M**

	Ans:	**(NOTE: If Students Solve This Bit For 3d Flip-flops Then Consider It)** **PN sequence generator using 4 D flip-flop is shown in following diagram:**	**2M Diagram**



PN sequence generator using 4 D flip-flop

Working:

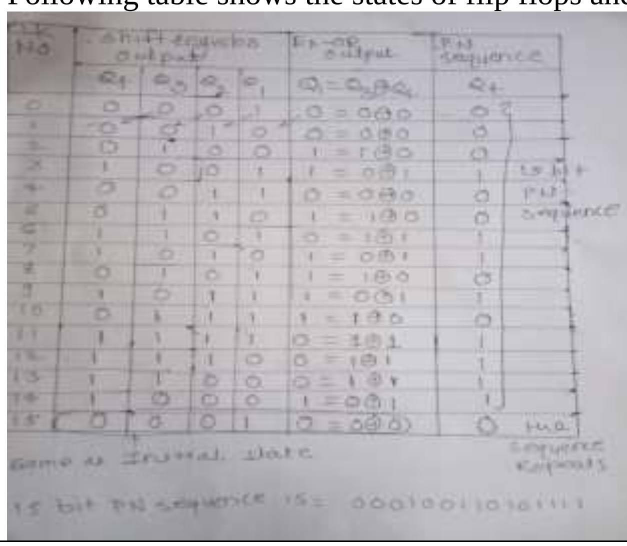
Maximum length of PN sequence "L" = 2^m-1 where m is number of D flip flops used.
Here D= 4 so L = 15 bits long

Input to first flip-flop is Q3⊕Q4 .the values of Q4 in successive state gives the PN sequence.

Assume initial contents of the flip flop be 1000,then with successive shifts the flip-flop contents will shift in to next flip flops

Following table shows the states of flip flops and output sequence for one period.

working 1M



No	Shift register output				Ex-OR output	PN sequence
	Q_4	Q_3	Q_2	Q_1	$Q_1 = Q_3 \oplus Q_4$	Q_4
0	0	0	0	1	0 = 0⊕0	0
1	0	0	1	0	0 = 0⊕0	0
2	0	1	0	0	1 = 1⊕0	0
3	1	0	0	1	1 = 0⊕1	1
4	0	0	1	1	0 = 0⊕0	0
5	0	1	1	0	1 = 1⊕0	0
6	1	1	0	1	0 = 1⊕1	1
7	1	0	1	0	1 = 0⊕1	1
8	0	1	0	1	1 = 1⊕0	0
9	1	0	1	1	1 = 0⊕1	1
10	0	1	1	1	1 = 1⊕0	0
11	1	1	1	1	0 = 1⊕1	1
12	1	1	1	0	0 = 1⊕1	1
13	1	1	0	0	0 = 1⊕1	1
14	1	0	0	0	1 = 0⊕1	1
15	0	0	0	1	0 = 0⊕0	0

15 bit PN sequence

Same as initial state

PN sequence repeats

15 bit PN sequence is= 000100110101111

Table 1M

	b)	**Attempt any ONE of the following:**	**6M**
	(i)	**Draw block diagram of DPSK transmitter and explain it's working. Draw W/F of given data (dt)=110101001101**	**6M**
	Ans:		**Diagram Operation Wave forms 2M Each**

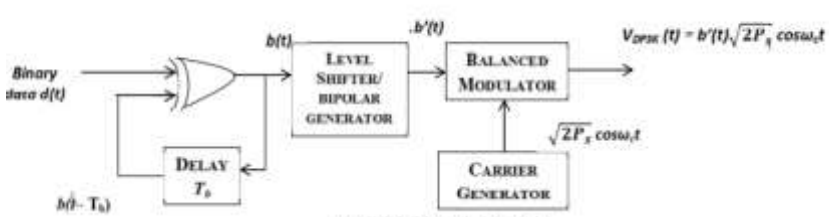


Figure : DPSK Transmitter

Principle :

It combines, differential encoding and phase shift keying. In BPSK receiver, the carrier recovery is done by squaring the received signal. Hence, when the received signal is generated by negative data bit, it is squared and thus we cannot determine if the received bit is –b(t) or b(t.) Hence DPSK is used to eliminate the ambiguity of the received bit

Operation

1] d (t) represents the data stream which is to be transmitted it is to one input of an EX-OR logic gate.

2] The EX-OR gate output "b (t)" is delayed by one bit period the applied to the other input of EX-OR gate.

3] The delayed represented by "b (t-Tb)". Depending on the values of "d (t)" and "b (t-Tb)" the EX-OR produces the output sequence "b (t)".The waveform for the generator .the waveform drawn by arbitrarily assuming that in the first interval b (0)=.

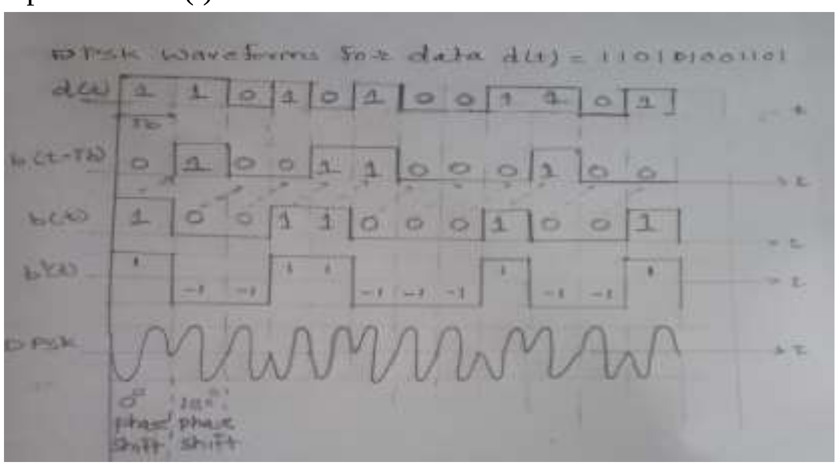
4] Output of EX-OR gate is the applied to a bipolar NRZ level which converts "b (t)" to a bipolar level "b(t) as shown

If b(t)=0 so b'(t) =- 1 and If b(t)=1 so b'(t) =+ 1

+1 VDpsk(t)= √ (2Ps) cosωt

That Means no phase Shift has been introduced

But when b (t) = 0, b' (t) = -1 Hence VDpsk (t)= -√ (2Ps) cosωt Thus 180^0 Phase shift is introduced to represent b (t) =0



(ii)	**Draw and explain PCM transmitter with neat block diagram and its waveform.**	**6M**
Ans:	PCM Transmitter Diagram	**Diagram Operation Wave forms 2M Each**

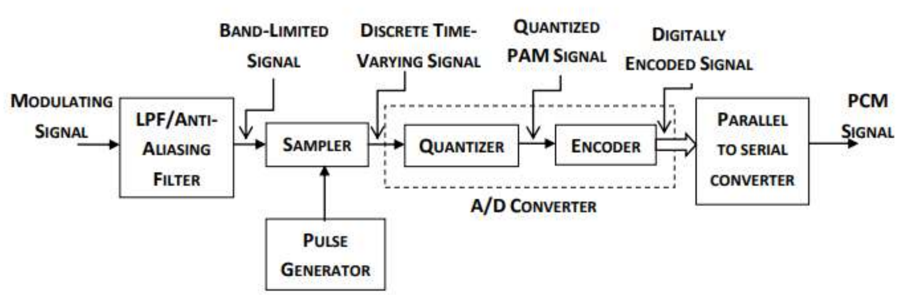


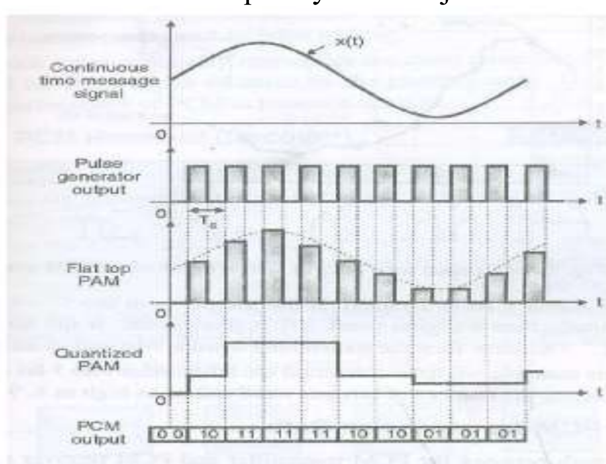
Fig. block diagram of PCM Transmitter

Explanation :

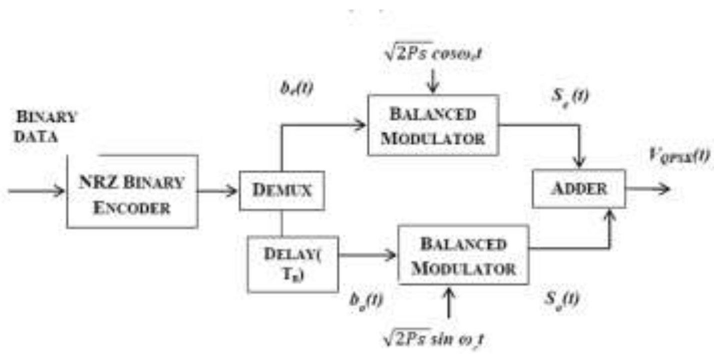
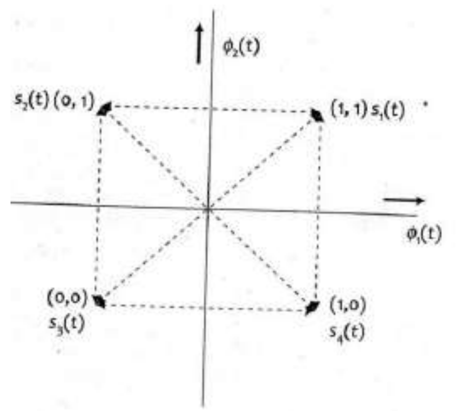
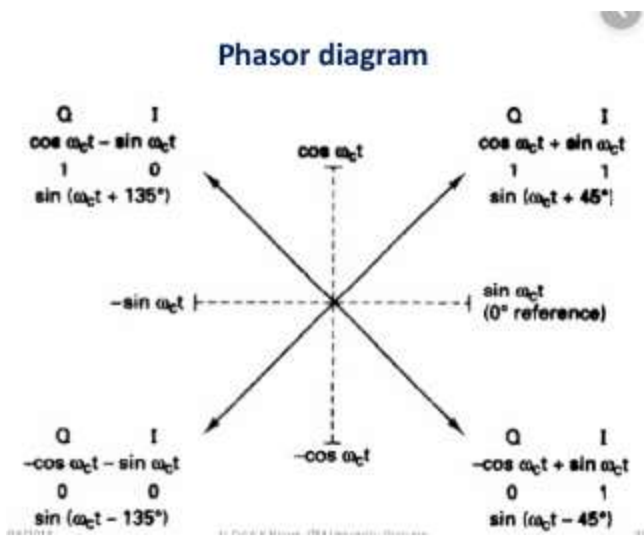
PCM Transmitter :

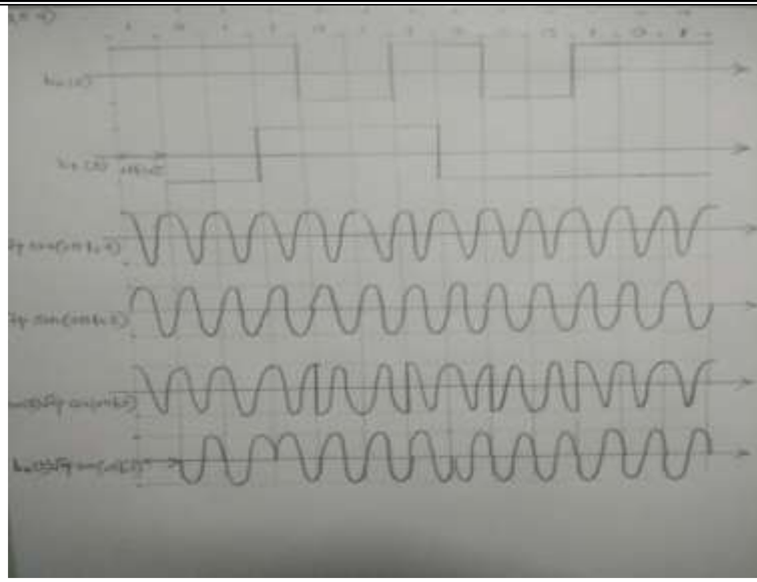
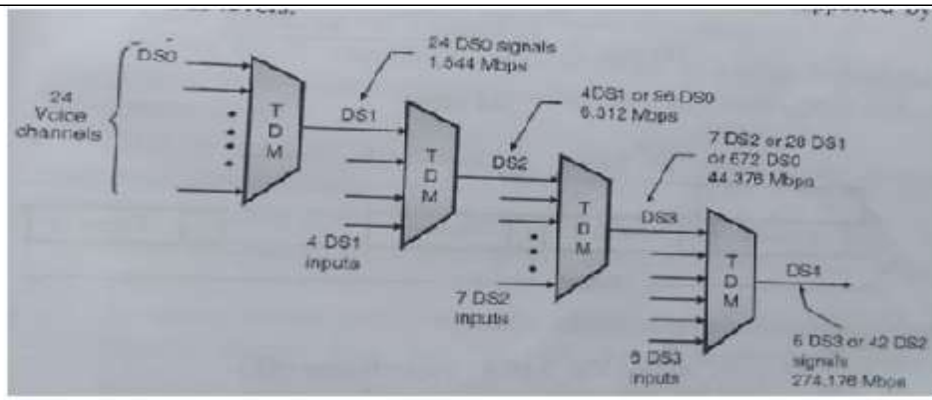
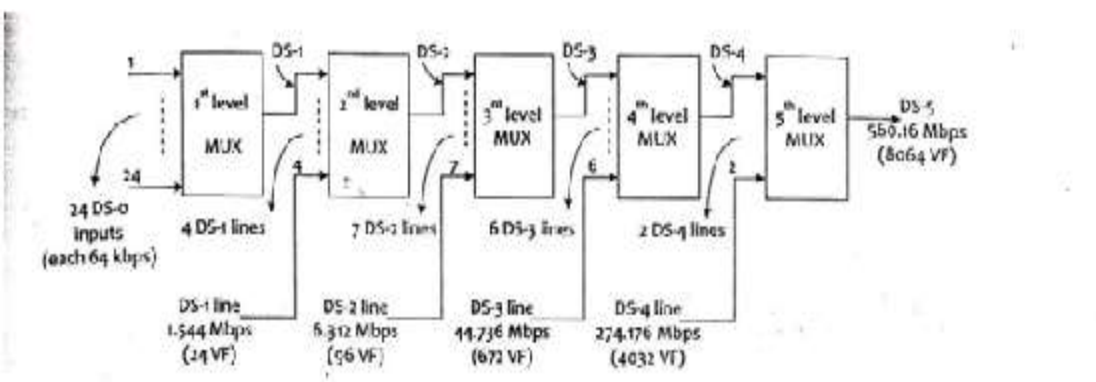
• The analog signal/modulating signal x (t) is passes through band limiting / low pass filter, which has a cut-off frequency fc=W Hz. This will ensure x (t) will not have any frequency component higher than "W". In other words, suppresses high frequency components and passes only low frequency signal to avoid 'aliasing error'.

- The band limited analog signal is then applied to sampled and hold circuit where this circuit acts as modulator and both modulating input signal and sampling signal with adequately high sampling rate are inputs to this circuit. Output of sampled and hold block is a flat topped PAM signal.
- These samples are subjected to operation "quantization" in the "quantizer". Quantization is a process of approximation of the value of respective sample into a finite number that will reduce data bits. The combined effect of sample and quantization produces is 'Quantized PAM' at the quantizer output.
- The Quantized PAM output is analog in nature. So to transmit it through digital communication system the quantized PAM pulses are applied to an encoder which is basically A to D convertor. Each quantized level is converted into N bit digital word by A to D converter.
- The communication system is normally connected to each other using a single cable i.e. serial communication. But the output of ADC is parallel which cannot be transmitted through serial communicating links. So this block will convert the parallel data into serial stream of data bits.
- A pulse generator produces train of rectangular pulses of duration "t" seconds. This signals acts as sampling signals for the sample and hold block. The same signal acts as "clock" signals for parallel to converter .the frequency "f" is adjusted to satisfy the criteria.



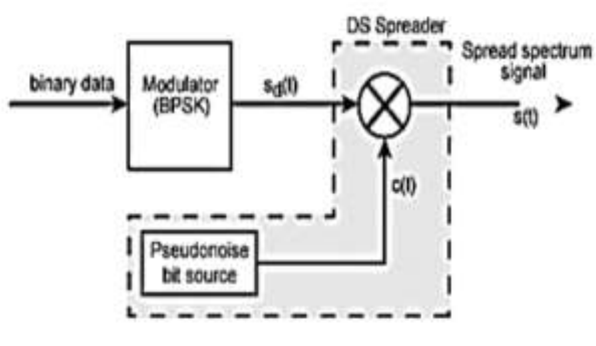
Q.5		**Attempt any TWO of the following:**	**16M**
	a)	**Draw QPSK modulator block diagram. Explain with constellation diagram and phasor diagram and draw its waveform of given data.d(t)=1011011000101.**	**8M**

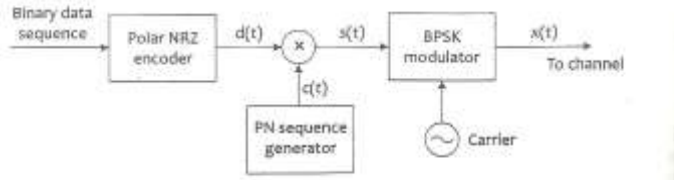
	Ans:	 **QPSK Modulator Block Diagram**  **Constellation diagram**  	**2M QPSK Modulator block diagram** **2M constellation and phasor diagram of QPSK** **4M**

			Waveform
	b)	**Explain North American digital multiplexing hierarchy with neat diagram.**	8M
	Ans:	 **OR** 	4M diagram
		Explanation: The first digital signal in true sense is the PCM voice signal. A PCM voice signal represents 64kbits/sec. i.e. 8000 sample /second* 8 bits per samples. Such a signal is called as digital signal at level zero (DS0). It is also called as T1 signal. Due to 8ooo sample/second, sampling rate, the time duration between adjacent samples will be 125 µsec. But practically DS0 signal is not transmitted because most of the telephone lines are analog. Hence in telephone central office, the subscriber analog line is passed through an anti-aliasing filter.	4M Explanation

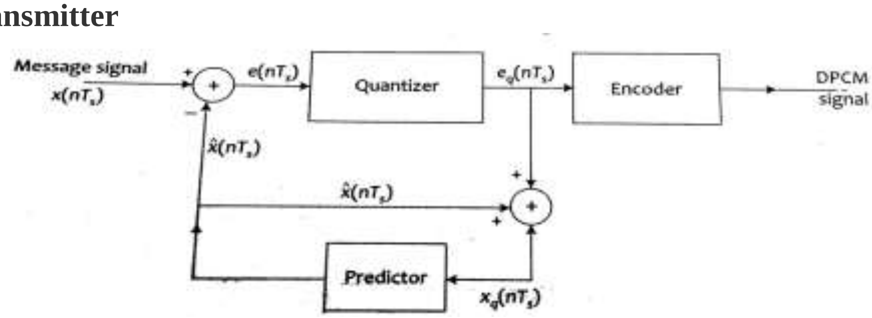
		The band limited signal is applied to a codec, which convert it into DS0 signal.24 DS0 lines are multiplexed into a DS1.The telephone companies implement TDM through the hierarchy of digital signals. This is called as digital signal service. Multiplexed signal is converted into a frame at the DS1 or T1 level.	
	c)	**State importance of spread spectrum modulation. List out application of spread spectrum modulation.(any two)**	**8M**
	Ans:	**Following are the Importance of spread spectrum −** • Cross-talk elimination • Better output with data integrity • Reduced effect of multipath fading • Better security • Reduction in noise • Co-existence with other systems • Longer operative distances • Hard to detect • Not easy to demodulate/decode • Difficult to jam the signals	**4M (1M Each point)**
		Applications: 1. Military application-resistance to jamming. 2. Secure Communication 3.CDMA in satellite communication 4.Police radar can employ spread spectrum to avoid detection by detectors employed by drives 5.Low density power spectra for signal hiding 6.LAN 7.GPS 8.Multipath rejection in ground based mobile station	**4M(2M each point)_**
Q.6		**Attempt any FOUR of the following :**	**16M**
	a)	**Compare QPSK and QAM(four points)**	**4M**
	Ans:	(table below)	**1M each for correct comparison point (Any 4 correct points)**

parameter	**QAM**	**QPSK**
1.Information is transmitted by change in	Amplitude and phase	phase
2.Number of bits/symbol	N=3 Or 4 Or 5 & so on	N=2
3.Number of possible symbols	$M=2^N$	Four
4.Detection method	coherent	coherent
5.minimum bandwidth	2fb/N	fb
6.symbol duration	NTb	2Tb
7.Type of modulation	Quadrature amplitude and phase modulation	Quadrature phase modulation
8.Location of signal points	Equally spaced and placed symmetrically about origin	On the circumference of the circle
9.Noise immunity	Better than QPSK	Comparatively less than QAM

		10.System complexity | More complex than QPSK | Less complex than QAM 11.Probability of error | Less than QPSK | More than QAM 12.Performance of system | Better than QPSK | Less than QAM	
	b)	**Explain specification of T carrier system.**	**4M**
	Ans:	1. Leased lines come in two configurations T1 and T3. A T1 line offers a data transfer rate of 1.54 million bits per second. 2. A T1 line is a dedicated connection meaning that it is permanently connected to the internet. 3. This is useful for web server or other computers that need to be connected to the internet all the time. 4. It is possible to lease only a portion of a T1 line using one of two systems fractional T1 or Frame relay. 5. You can lease them in blocks ranging from 128 kbps to 1.5 Mbps. 6. The differences are not worth going into in detail but fractional T1 will be more expensive at the slower available speeds and frame relay will be slightly more expensive as you approach the full T1 speed of 1.5 Mbps. 7. AT3 line is significantly faster at 45million bits per second. 8. Leased lines are expensive and are generally used only by companies whose business is built around the internet or need to transfer massive amounts of data.	**4M for correct specifications**
	c)	**Explain Direct Sequence Spread Spectrum techniques with the help of block diagram.(DSSS)**	**4M**
	Ans:	**DSSS(Direct Sequence Spread Spectrum):** • Each bit is represented by multiple bits using spreading code, Spreading code spreads signal across wider frequency band and in proportion to number of bits used, • e.g., 10 bit spreading code spreads signal across 10 times bandwidth of 1 bit code • One method: Combine input with spreading code using XOR a. Input bit 1 inverts spreading code bit b. Input zero bit doesn't alter spreading code bit. • Data rate is equal to original spreading code and performance is similar to FHSS  DSSS Transmitter OR	**2M for diagram and 2M for explanation**

<table>
<tr><td></td><td></td><td>


The generation block diagram of DPSK signal is shown in Figure 3.16. The data stream to be transmitted, *d(t)*, is applied to one input of an exclusive-OR logic gate. To the other gate input the output of the exclusive-OR gate *b(t)* delayed by time T_b allocated to one bit is applied. This second input is then $b(t - T_b)$.
</td><td></td></tr>
<tr><td></td><td>d)</td><td>Explain DPCM transmitter with neat block diagram.</td><td>4M</td></tr>
<tr><td></td><td>Ans:</td><td>
DPCM Transmitter



- DPCM system is particularly efficient when there is high correlation between adjacent samples. In video and audio transmission, the information signal does not rapidly change from one sample to the other.
- These highly correlated samples are encoded using standard PCM system, the resultant encoded signal contains *redundancy* (repeated code-words are transmitted) which leads to larger bandwidth utilization in PCM. Before encoding, this redundancy can be removed.
- Correlation between the adjacent samples suggests that it should be possible to predict the present value of the message signal from the knowledge of its immediate past behavior.
- The DPCM system employs a predictor which predicts the present sample value making use of immediate past samples.
- If the prediction is good the difference between the actual value and predicted value, called the error will have a smaller dynamic range than the original message itself and therefore needs far fewer bits per each error sample than that would have required for the original sample.
</td><td>2M for diagram

2M for explanation</td></tr>
<tr><td></td><td>e)</td><td>State Shannon's Hartleystheorem.What is Shannon's information rate theoretically?</td><td>4M</td></tr>
<tr><td></td><td>Ans:</td><td>
Shannon Hartley Theorem:

The channel capacity of a white, band limited Gaussian channel is given by,

$$C = B \log_2 \left(1 + \frac{S}{N}\right) \quad \text{bit/sec}$$

Where, B = Channel Bandwidth
S = Signal Power
N = Noise within the channel bandwidth
</td><td>2M for Theorem and

2M for</td></tr>
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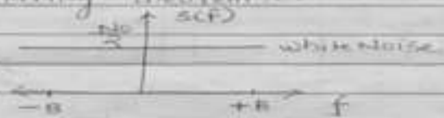
Shannon Hartley theorem :—


where $N = \int_{-B}^{B} \frac{N_o}{2} df = \frac{N_o}{2}(2B) = N_o B$
$\therefore C = B \log_2\left(1 + \frac{S}{N_o B}\right)$
To Calculate max Possible capacity:-
$\lim_{B\to\infty} C = \lim_{B\to\infty} B \log_2\left(1 + \frac{S}{N_o B}\right)$
$C_\infty = \lim_{B\to\infty} B \frac{N_o}{S} \frac{S}{N_o} \log_2\left(1 + \frac{S}{N_o B}\right)$
$= \lim_{B\to\infty} \frac{S}{N_o} \log_2\left(1 + \frac{S}{N_o B}\right)^{\frac{N_o B}{S}}$
$= \lim_{B\to\infty} \frac{S}{N_o} \log_2\left(1 + \frac{S}{N_o B}\right)^{\frac{1}{\frac{S}{N_o B}}}$
Let $x = \frac{S}{N_o B}$
as $B \to \infty$, $x \to 0$
$= \lim_{x\to 0} \frac{S}{N_o} \log_2 (1+x)^{\frac{1}{x}}$
$= \frac{S}{N_o} \log_2 \lim_{x\to 0} (1+x)^{\frac{1}{x}}$
$= \frac{S}{N_o} \log_2 e$
$\left\{ \lim_{x\to 0} (1+x)^{\frac{1}{x}} = e \right\}$
$C_\infty = 1.44 \frac{S}{N_o}$
This is shannon’s information rate theoretically.
</td>
<td>shannon’s information rate</td>
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