(ISO/IEC - 2700

WINTER – 19EXAMINATIONS

Subject Name: Microcontroller and Applications Model Answer Subject Code:

Important Instructions to examiners:

- 1) The answers should be examined by key words and not as word-to-word as given in themodel answer scheme.
- 2) The model answer and the answer written by candidate may vary but the examiner may try to assess the understanding level of the candidate.
- 3) The language errors such as grammatical, spelling errors should not be given moreImportance (Not applicable for subject English and Communication Skills.
- 4) While assessing figures, examiner may give credit for principal components indicated in the figure. The figures drawn by candidate and model answer may vary. The examiner may give credit for anyequivalent figure drawn.
- 5) Credits may be given step wise for numerical problems. In some cases, the assumed constant values may vary and there may be some difference in the candidate's answers and model answer.
- 6) In case of some questions credit may be given by judgment on part of examiner of relevant answer based on candidate's understanding.
- For programming language papers, credit may be given to any other program based on equivalent concept. 7)

Q. No.	Sub Q. N.	Answer					
							Scheme
Q.1	(A)	Attempt any <u>THREE</u> of the foll	owing:				12- M
	a)	Draw symbol of NAND gate and	write it	s truth	table.		4 M
	Ans:	Symbol:					Symbol
				NAND	y = A . B		:2M Truth
		Truth Table:	ЪЦ				Table:
			Inp	uts	Output		2M
			Α	В	Υ =A . B		
			0	0	1		
			1	0	1		
			1	1	0		
		State function of following pins	of 16*2]	LCD.		1	
		(i) RS					
	b)	(ii) R / W					4M
		(iii)EN					
		(iv)LED+					
	Ans:	RS: RS is the register select pin us	ed to wr	ite disp	lay data to th	e LCD (characters), this pin	1M
		hasto be high when writing the dat	a to the	LCD. I	During the ini	tializing sequence and other	each
		commands this pin should be low.					
		R/W: Reading and writing data to $(R/W-1)$ to write the data to I/CD	the LCD), for re	adding the dat	a R/W pin should be high V_{-0}	
		EN: Enable pin is for starting or en	nabling f	he mod	ule. A high t	o low pulse of about 450ns	
		Pulse is given to this pin. Sends da	ta to dat	a pins v	when a high t	o low pulse is given at this	
		pin.		-	2		

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	iv) LED + It is pin no 15, inputpin.	Backlight LED pin	positive te	rminal.				
c)	List any four C data types with its size and ranges.							
Ans:	Data Ty	pe Size in	Bits	Data Range/Usage		1M		
	Unsigned o	har 8-b	it	0 to 255		each		
	Signed ch	ar 8-b	it	-128 to + 127				
	Unsigned	int 16-b	oit	0-65535				
	signed ir	nt 16-b	oit	-32768 to + 32767				
	sbit	1-b	it	SFR bit-addressable only				
	bit	1-b	it	RAM bit-addressable only				
	sfr	8-b	it	RAM addresses 80 –FFH only				
d)	(i) RST (ii) PSEN (iii)RXD (iv)EA					4M		
Ans:	(i) RST		_			1M		
	It is a RESET pin, which	ch is used to reset th	ne microcon	troller to its initial values.		each		
	It is active low output co it is activated every six (iii)RXD Serial input line (Receiv	ontrol signal used to oscillator periods w e).RXD pin is pin r	o activate en while reading no 10 and in	able signal of external ROM g the external memory. put pin to the microcontrolle	/ EPRM r. It is	hu		
	used to input serial data	to the microcontrol	ler.					
	It is active low output co program memory when	ontrol signal. When EA =0, μc accesses	$EA = 1, \mu c$ only extern	accesses internal and externational program memory.	ıl			
(B)	Attempt any <u>ONE</u> of t	he following:	2			6M		
a)	State alternate function	ns of Port 3.				2M		
, u)								

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 			,		
Ans:		P3 BIT	FUNCTION		
		P3.0	RXD		
		P3.1	TXD		
		P3.2	INTO		
		P3.3	INTI		
		P3.4	то		
		P3.5	TI	1	
		P3.6	WR		
		P3.7	RD		
• `	N				(3.6
b)	Describe address	sing modes of 8051 wi	th examples.		4M
Ans:	Addressing mode	es of 8051:			
	1.Immediate Add	ressing mode			
	2. Register Addre	ssing mode			
	3. Direct Address	ing mode			
	4 Register Indirec	t addressing mode			
	5.Indexed Addres	sing mode			
	1) Immediate Ad	dressing mode:		11 41	
	Immediate addres	sing simply means that	he wood	mows the	
	Eor example the i	de) is the data value to	be used.		
	For example the I $MOV \wedge #25U \cdot I$	and 25H into A			
	Moves the value C	2511 into the accumulat	or The # symbol talls the assemble	r that tha	
	immediate addres	sing mode is to be used	$\frac{1}{1}$		
	2) Register Add	ressing Mode.	1.		
	One of the eight of	eneral-registers R0 to	R7 can be specified as the instruct	ion Operand The	
	assembly languag	e documentation refers	to a register generically as Rn	ion operand. The	
	For example, inst	ruction using register a	ddressing is :		
	ADD A. R5 : Add	the contents of register	er R5 to contents of A (accumulator))	
	Here the contents	of R5 are added to the	accumulator. One advantage of reg	ister addressing	
	is that the instruct	ions tend to be short, s	ingle byte instructions.	U	
	3) Direct Addres	sing Mode:			
	Direct addressing	means that the data va	lue is obtained directly from the me	mory location	
	specified in the in	struction.			
	For example cons	ider the instruction:			
	MOV R0, 40H; S	ave contents of RAM l	ocation 40H in R0.		
	The instruction re	ads the data from Inter	nal RAM address 40H and stores th	is in theR0.	
	Direct addressing	can be used to access l	Internal RAM, including the SFR re	gisters.	
	4) Register Indir	ect Addressing Mode	:		
	In Indirect addres	sing mode, the data is	obtained from a memory location w	which is indirectly	
	An example instr	su ucuon. Iction which uses indi-	ract addressing is as follows:		
		OVA contents of DAM	location whose address is hold by D	() into A	
	The @ symbol in	dicated that the indirect	t addressing mode is used. If the dat	o into A	
		incated that the mullect	addressing mode is used. If the dat	a 15 11151UC	

		The CPU, only registers R0 & R1 are used for this purpose.	
		5) Indexed Addressing Mode:	
		With indexed addressing a separate register, either the program counter, PC, or the data	
		pointer DTPR, is used as a base address and the accumulator is used as an offset address.	
		The effective address is formed by adding the value from the base address to the value from	
		the offset address. Indexed addressing in the 8051 is used with the JMP or MOVC	
		instructions. Look up tables are easy to implement with the help of index addressing.	
		Consider the example instruction: MOVC A, @A+DPTR	
		MOVC is a move instruction, which moves data from the external code memory space. The	
		address operand in this example is formed by adding the content of the DPTR register to the	
		accumulator value. Here the DPTR value is referred to as the base address and the	
		accumulator value us referred to as the index address.	
Q.2		Attempt any <u>TWO</u> of the following:	16- M
		Write an ALP to find largest number from given array of 10 bytes in external RAM	ON /
	a)	location 2000h onwards. Store largest number in internal RAM location 40h.	81/1
		CLR PSW 3 · Select Bank () PSW 3	Correct
		MOV P1 0AH : Initialize byte counter	Correct
		MOV DTD # 2000H	program:
		DEC D1 , Initialize memory pointer DEC D1	8M
		MOV X A @DDTD I Load number in accumulator	
		MOV A A, @DPTK ; Load number in accumulator	
	A	MOV 40 H, A ; Store number in memory location	
	An	; Increment memory pointer by I	
	:	MOVXA, @DTPR ; Read next number	
		CJNE A, 40 H, DN ; if number≠ next number, and then go to NEX I	
		DN: JC NEXT ; If next number < number then go to NEXT	
		MOV 40H, A ; Else replace NEXT number with number	
		NEXT: DJNZ R1, UP ; Decrement byte counter by 1, if byte counter $\neq 0$	
		then go to UP	
		LOOP: AJMP LOOP ; Stop	
	b)	Draw interfacing diagram of DAC 0808 with 8051µC and write C program to generate	8M
	U)	triangular wave.	0111
	An		Diagram
		vcc	AM
	•		-+141
		Vref (+) 2.5k0	
		C2 Vref(-)	
		+vcc 0 P1.3 05 05 +15V	
		5 $p_{1,2}$ $p_{2,2}$ $p_{2,1}$ $p_{3,0}$	
		swy c I 8 3 + 4 Vo	
		GND	
		-	
		Lto V Convertor	

		#include <reg51.h></reg51.h>	
		void main(void)	
		{	
		unsigned char d:	
		while(1)	Program
		s s s s s s s s s s s s s s s s s s s	:4M
		$\int d_{-0} d_{-255} d_{++}$	• • • • • • •
		101(u=0, u<255, u++)	
		P1 = d;	
		for(d=255; d>0; d)	
		{	
		P1 = d;	
		}	
		}	
		}	
	c)	Draw the interfacing diagram of stepper motor with 8051. Write excitation code to rotate	8M
		it in clockwise direction.	
	Ans	+5V +5V +5V	Diagram:
	:		6M
		Reset 10 JULF/10V 9 RST Stepper Motor	Code:2M
		P1.0 1 16 A1	
		$\begin{array}{ c c c c c c c c c c c c c c c c c c c$	
		X1=11.0592 MHz 20	
		+ +	
		Clearlying Store # Wile Hard Wile Hard D. Wile Hard C. Wile Hard D.	
		Clockwise Step # winding A winding B winding C winding D	
		$\frac{1}{2}$ $\frac{1}{1}$ $\frac{1}{1}$ $\frac{1}{1}$ $\frac{1}{1}$ $\frac{1}{1}$ $\frac{1}{1}$	
		$\frac{2}{2}$ 0 1 0 0	
		$\frac{3}{4}$ 0 0 1 1 0	
		$\mathbf{Y} \stackrel{4}{\longrightarrow} \stackrel{0}{\longrightarrow} \stackrel{0}{\longrightarrow} \stackrel{1}{\longrightarrow} \stackrel{1}{\longrightarrow}$	
		•	
0.1			10.35
Q.3		Attempt any <u>FOUR</u> of the following:	12- M
			414
	a)	Draw and explain Reset circuit of 8051µC.	41 VI

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A :	Ans	Power on & manual reset circuit	2 marks: circuit diagram
		The power on reset circuit consists of 8.2 KΩ resistor and 10 µF capacitor. The values of these components are sufficient to provide a delay to make RST pin high for two machine cycles. For manual reset function switch is provided. Upon power ON or Key Press the RST pin goes HIGH and as capacitor charges through resistor R, RST signal goes LOW. This generates active high reset signal for specific time decided by values of R & C.	2marks : explanati on
b)	Describe mode 2 of timer. State application of it.	4M
A :	Ans	Mode 2 – 8 bit Auto Reload TL operates as an 8-bit Timer / counter.TH holds a reload value. When TL overflows (Reached FFH), the TFx flag is set, TL is reloaded from the value in TH and counting continues. Pulse Input TLX8Bits TFX Interrupt Reload TLX THX8Bits THX8Bits TO generate baud rate in serial communication	3Marks: mode 2 descripti on 1mark : applicati on
C	2)	Write C program to toggle bits of P2. Use software delay.	4M
A :	Ans	<pre>#include <reg51.h> void delay(unsigned int); void main(void) { P2=0X00; // PORT 2 as output port while(1) { P2=0X00; delay(200); P2=0XFF; delay (200); } } void delay(unsigned int t) { }</reg51.h></pre>	4M for correct program) Any amount of delay can be considere d

\ns)	9) Convert $(59)_{10} = (?)_{16}$ (2 morres) 16 $ _{3}^{59}$ 11 $=(B)_{16}$ \therefore (59) $_{10} = (3B)_{16}$ b) $(3B)_{16} = (?)_{2}$ (2 morres) \vdots (3B) $_{16} = (?)_{2}$ (2 morres) \vdots (3B) $_{16} = (011 + 011)_{2}$ Draw the format of SCON SFR.	4M					
NNS	9) Convide $(59)_{10} = (?)_{16}$ (2 morros) $16 59 11 = (B)_{16}$ $3 = (3)_{16}$ $(. (59)_{10} = (3B)_{16}$ $(. (3E)_{16} = (?)_{2}$ (2 mark) $3 B (. (1011)_{2})$ $(. (3B)_{16} = (0011 + 011)_{2}$						
ns	a) Convert $(59)_{10} = (?)_{16}$ $16 59 11 = (B)_{16}$ $16 59 11 = (B)_{16}$ $3 = (3)_{16}$ $(59)_{10} = (3B)_{16}$ $(2 \mod K)$ b) $(3E)_{16} = (?)_2$ $(2 \mod K)$						
ns	a) Convert $(59)_{10} = (?)_{16}$ $16 59 11 = (B)_{16}$ $3 = (3)_{16}$ $(59)_{10} = (3B)_{16}$						
ns	a) Convert $(59)_{10} = (?)_{16}$ $16 59 11 = (B)_{16}$ $3 = (3)_{16}$						
ns	a) Convilt (59)10 = (?)16 - (2 marins)						
)	Convert $(59)_{10} = (?)_{16} = (?)_2$.	4 M					
	IOP(J=0;J<=1275;J++); } ANY OTHER CORRECT PROCEMM LOGIC SHOULD BE GIVEN MARKS						
	for(i=0;i<=t;i++)						
	{						
	<pre>} void delay(unsigned int t)</pre>						
	delay(200);						
	{ P2= ~ P2;						
	P2=0X00; // PORT 2 as output port while(1)						
	<pre>void main(void) {</pre>						
	<pre>#include <reg51.h> void delay(unsigned int); </reg51.h></pre>						
	OR						
	for(j=0;j<=1275;j++);						



Q.4	(A)	Attempt any <u>THREE</u> of the following :	12- M
	a)	Draw interfacing diagram for temperature measurement using LM 35, ADC 0808 with 8051 microcontroller.	4M
	Ans :	³⁰ <i>p</i> ^F <i>f</i> ¹ <i>μ</i> ¹	Correct diagram 4M
	b)	Explain bitwise shift operator with example.	4M
	Ans :	Bitwise Left Shift Operator in C : << [variable]<<[Number of Places] $P0=0x_3C<<2$ After execution of this instruction Shift number 2 bits wheft: $3C = 0011 \ 1100$ 1^{st} left shift = 0111 1000 2^{nd} left shift = 1111 0000 So, $P0=0xF0$ Bitwise Right Shift Operator in C: >> [variable]>>[number of places] $P0=0x_3C >> 2$ After execution of this instruction Shift number 2 bits to Right: $3C=0011 \ 1100$ 1^{st} right shift = 0001 1110 2^{nd} right shift = 0000 1111 8_{s} P0 $0x_2C$	2marks: left shift operator explanati on 2marks: Right shift operator explanati on
	c)	Subtract (25) ₁₀ from (52) ₁₀ using 2's compliment method.	4M

1 1115				$(52)_{10} - (25)_{10}$	
:			($(1000)_{2}$ $(1000)_{2}$	
			ی ^{ار} م ا ^{رد} کار	$25)_{10} = (11001)_{2}$ $= 110001$ $= 011001$ $= 1^{1500} \text{ mplement of } (011001) = 1^{1500} \text{ mplement of } (011001) = 100110$ $= \pm 1$ $= \pm 1$ 1001101 $= \pm 1$ 100111 $= \pm 1$ 100111 $= \pm 1$ 100111 $= \pm 1$ $= \pm$	
d)	Draw the	e forma	t of TC	$\therefore (011011)_2 = (27)_{10}$ $\therefore (52)_{10} = (27)_{10}$ CON sfr and explain each bit.	4M
Ans	то	CON: TI	MER/C	OUNTER CONTROL REGISTER.	Format-2
Ans :	т	CON: TI	MER/C	TF0 TR0 IE1 IT1 IE0 IT0	Format-2 marks Function
Ans :	TF1	TF1 TCOM	MER/C TR1	TF0 TR0 IE1 IT1 IE0 IT0 ner 1 overflow flag. Set by hardware when the Timer/Counter 1 overflows. Cleared by hardware as occessor vectors to the interrupt service routine.	Format-2 marks Function - 2marks
Ans :	TF1 TR1	TF1 TCON	MER/C TR1 V.7 Tin pro	TFO TRO IE1 IT1 IE0 IT0 ner 1 overflow flag. Set by hardware when the Timer/Counter 1 overflows. Cleared by hardware as occessor vectors to the interrupt service routine. ner 1 run control bit. Set/cleared by software to turn Timer/Counter 1 ON/OFF.	Format-2 marks Function - 2marks
Ans :	TF1 TR1 TF0	TF1 TCON TCON TCON	MER/C TR1 V.7 Tin prc V.6 Tin V.5 Tin prc	TFO TRO IE1 IT1 IE0 IT0 ner 1 overflow flag. Set by hardware when the Timer/Counter 1 overflows. Cleared by hardware as ocessor vectors to the interrupt service routine. Interrupt service routine. ner 1 run control bit. Set/cleared by software to turn Timer/Counter 1 ON/OFF. Interrupt service routine. ner 0 overflow flag. Set by hardware when the Timer/Counter 0 overflows. Cleared by hardware as ocessor vectors to the service routine.	Format-2 marks Function - 2marks
Ans :	TF1 TR1 TF0 TR0	TF1 TCON TCON TCON TCON	MER/C TR1 V.7 Tin pro V.6 Tin pro V.5 Tin pro	TFO TRO IE1 IT1 IE0 IT0 ner 1 overflow flag. Set by hardware when the Timer/Counter 1 overflows. Cleared by hardware as ocessor vectors to the interrupt service routine. It1 It1 It1 It1 It1 It1 ner 1 overflow flag. Set by hardware when the Timer/Counter 1 overflows. Cleared by hardware as ocessor vectors to the interrupt service routine. It1 It	Format-2 marks Function - 2marks
Ans :	TF1 TR1 TF0 TR0 IE1	TF1 TCON TCON TCON TCON TCON	MER/C TR1 V.7 Tin pro V.6 Tin V.5 Tin pro V.4 Tin V.3 Ex han	COUNTER CONTROL REGISTER. TF0 TR0 IE1 IT1 IE0 IT0 Inter 1 overflow flag. Set by hardware when the Timer/Counter 1 overflows. Cleared by hardware as beessor vectors to the interrupt service routine. mer 1 run control bit. Set/cleared by software to turn Timer/Counter 1 ON/OFF. mer 0 overflow flag. Set by hardware when the Timer/Counter 0 overflows. Cleared by hardware as beessor vectors to the service routine. mer 0 run control bit. Set/cleared by software to turn Timer/Counter 0 ON/OFF. mer 0 run control bit. Set/cleared by software when External Interrupt edge is detected. Cleared by rdware when interrupt is processed.	Format-2 marks Function - 2marks
Ans :	TF1 TR1 TF0 TR0 IE1 IT1	TF1 TCON TCON TCON TCON TCON TCON	MER/C TR1 V.7 Tin pro V.6 Tin pro V.4 Tin V.3 Ex hai V.2 Inte	COUNTER CONTROL REGISTER. TF0 TR0 IE1 IT1 IE0 IT0 Inter 1 overflow flag. Set by hardware when the Timer/Counter 1 overflows. Cleared by hardware as occessor vectors to the interrupt service routine. mer 1 run control bit. Set/cleared by software to turn Timer/Counter 1 ON/OFF. Inter 0 overflow flag. Set by hardware when the Timer/Counter 0 overflows. Cleared by hardware as occessor vectors to the service routine. mer 0 run control bit. Set/cleared by software to turn Timer/Counter 0 ON/OFF. Interrupt 1 edge flag. Set by hardware when External Interrupt edge is detected. Cleared by rdware when interrupt is processed. terrupt 1 type control bit. Set/cleared by software to specify falling edge/low level triggered External terrupt.	Format-2 marks Function - 2marks
Ans :	TF1 TR1 TF0 TR0 IE1 IT1 IE0	TF1 TCON TCON TCON TCON TCON TCON TCON	MER/C TR1 V.7 Tin pro V.6 Tin V.5 Tin V.4 Tin V.3 Ext V.2 Internet V.2 Internet V.1 Ext	COUNTER CONTROL REGISTER. TF0 TR0 IE1 IT1 IE0 IT0 Inter 1 overflow flag. Set by hardware when the Timer/Counter 1 overflows. Cleared by hardware as occessor vectors to the interrupt service routine. mer 1 run control bit. Set/cleared by software to turn Timer/Counter 1 ON/OFF. Interrupt 0 overflow flag. Set by hardware when the Timer/Counter 0 overflows. Cleared by hardware as occessor vectors to the service routine. mer 0 run control bit. Set/cleared by software to turn Timer/Counter 0 ON/OFF. Interrupt 1 edge flag. Set by hardware when External Interrupt edge is detected. Cleared by rdware when interrupt is processed. terrupt 1 type control bit. Set/cleared by software to specify falling edge/low level triggered External terrupt. terrupt 1 type control bit. Set/cleared by software when External Interrupt edge detected. Cleared by rdware when External Interrupt edge detected. Cleared by rdware when interrupt 0 edge flag. Set by hardware when External Interrupt edge detected. Cleared by rdware when interrupt is processed.	Format-2 marks Function - 2marks
Ans :	TF1 TR1 TF0 TR0 IE1 IT1 IE0 IT0	TF1 TCON TCON	MER/C TR1 V.7 Tin pro V.6 Tin pro V.5 Tin pro V.4 Tin V.3 Ex har V.2 Inte Inte V.1 Ex har V.1 Ex har	TFO TRO IE1 IT1 IE0 IT0 mer 1 overflow flag. Set by hardware when the Timer/Counter 1 overflows. Cleared by hardware as ocessor vectors to the interrupt service routine. Immer 1 run control bit. Set/cleared by software to turn Timer/Counter 1 ON/OFF. mer 0 overflow flag. Set by hardware when the Timer/Counter 0 overflows. Cleared by hardware as ocessor vectors to the service routine. Immer 0 overflow flag. Set by hardware when the Timer/Counter 0 overflows. Cleared by hardware as ocessor vectors to the service routine. mer 0 run control bit. Set/cleared by software to turn Timer/Counter 0 ON/OFF. Immer 0 run control bit. Set/cleared by software when External Interrupt edge is detected. Cleared by rdware when interrupt is processed. werrupt 1 type control bit. Set/cleared by software to specify falling edge/low level triggered External errupt. ternal Interrupt 0 edge flag. Set by hardware when External Interrupt edge detected. Cleared by rdware when interrupt is processed. ternupt. ternupt 0 type control bit. Set/cleared by software to specify falling edge/low level triggered External errupt. ternupt 0 type control bit. Set/cleared by software to specify falling edge/low level triggered External errupt.	Format-2 marks Function - 2marks
Ans : (B)	тс ТF1 ТR1 ТF0 ТR0 IE1 IT1 IE0 IT0 Аttempt	TF1 TCON: TI TCON TCON TCON TCON TCON TCON TCON	MER/C TR1 V.7 Tin pro V.6 Tin pro V.4 Tin V.3 Ex har V.2 Inte Inte V.1 Ex har V.1 Ex har V.1 Inte NE of t	TFO TRO IE1 IT1 IE0 IT0 ner 1 overflow flag. Set by hardware when the Timer/Counter 1 overflows. Cleared by hardware as ocessor vectors to the interrupt service routine. It10 It10 ner 1 run control bit. Set/cleared by software to turn Timer/Counter 1 ON/OFF. It10 It10 It10 ner 0 overflow flag. Set by hardware when the Timer/Counter 0 overflows. Cleared by hardware as ocessor vectors to the service routine. It10 It10 ner 0 run control bit. Set/cleared by software to turn Timer/Counter 0 ON/OFF. It10 It10 It10 terrupt 1 edge flag. Set by hardware when External Interrupt edge is detected. Cleared by rdware when interrupt is processed. It10 It10 It10 terrupt 1 type control bit. Set/cleared by software to specify falling edge/low level triggered External terrupt. It10 It10 It10 terrupt 1 type control bit. Set/cleared by software to specify falling edge/low level triggered External terrupt. It10 It10 It10 It10 terrupt 0 type control bit. Set/cleared by software to specify falling edge/low level triggered External terrupt. It10 I	Format-2 marks Function - 2marks 6M



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	Ans :	One T-state is the time period of one clock signal. It is the reciprocal of system clock frequency. Machine cycle is the minimum time taken by microcontroller to perform an operation. One machine cycle has 6 states. One state is 2 T-states. Therefore one machine cycle is 12 T-states. Time to execute an instruction, called instruction cycle is found by multiplying C by 12 and dividing product by Crystal frequency. T=(C*12)/crystal frequency Where C is number of machine cycles	Explanat ion: 2 marks each.
	b)	Explain stack memory. Write any two stack related instruction.	6M
	Ans :	 The stack memory is part of RAM used by the CPU to store information temporarily. This information may be either data or address. The CPU needs this storage area as there are only a limited amount of registers. The register used to access stack memory is called stack pointer. Upon reset SP contains 07H; this causes the stack to begin to location 08H. So, Register banks 2, 3, 4 (08H to 1FH) form the default stack area. The stack is generally placed in the general-purpose area (30H to 7FH) of the internal RAM. Stack Related Instructions: (any two) PUSH POP CALL (ACALL, LCALL) RET 	4 marks: Stack memory explanati on Writing Any two instructio ns: 2 marks: (1 mark each instructio n)
Q.5		Attempt any <u>TWO</u> of the following :	16- M
	a)	Write C program to transmit 'MSBTE' on TXD line.	8M
	Ans :	Baud Rate Calculation: Timer Value = $\frac{2^{SMOD} \times Oscfreq}{12 \times 32 \times \text{Re quired Baud rate}}$ Considering SMOD = 1	2Marks for Calculati on



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	$2^0 \times Oscfreq$	
Timer Value	= 12 × 32 × Re quired Baud rate	
Oscfreq = 11.	0592Mhz	
	11.059 <i>Mhz</i>	
T ' V 1	$12 \times 32 \times \text{Re quired baud rate}$	
1 imer Value = Case - 1 Re	= and $=$ 4800	
	Junea Dava Fale 1000	
	28,800	
	4800	
Time value =	4000	
Timer value =	= 6	
- 6 must be lo	oaded in Timer for Required Delay.	
Case – 2) Rec	uired Baud rate =9600	
Timer value =	= 28,800 / 9600	
Timer value =	= 3	
-3 must be lo	aded in Timer for Required Delay	1 Mor
<u>C Program:</u>		for
#include <re< td=""><td>G51.h></td><td></td></re<>	G51.h>	
void Trans(un	Isigned char X);	calcula
void main(voi	(1)	n and
$\begin{bmatrix} 1 \\ TMOD - 0X' \end{bmatrix}$	20.	For
TH13	// for 9600 Baud rate	Progra
SCON = 0X5	0·	
TR1 = 1:	~,	
while(1)		
{		
	<pre>Frans(` `);</pre>	
	Trans('M');	
r	Trans('S');	
, r	Trans('B');	
,	Trans('T');	
, 	Trans('E');	
}		
void Trans(un	isigned char x)	
SBUF =	X;	
while(11	z = z = 0	
}		
Write an AL	P to generate square wave of 1kH_{-} frequency on n2.3. Use timer 1 in	8M
,, 1100 un AL.	- 10 MII	

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				2Marks
	Simulator	C - Editor		
				Diagram
	Emulator	Simulator		
	Logic Analyzer	Cross Assembler		
	Target system performance Evaluator	RTOS		
. In Fuche data a sector		(]		6Marks
• In Embedded system	ns Code generation	number of latest so	ftware tolls like simulators	010101110
Logic Analyzers, pro	ofiler, Emulators etc.	number of fatest so	it ware tons like simulators,	Explanat
• When all of these p	rograms are integra	ted in one software	package then it is called as	ion
Integrated Developn	nent environment (II	DE)		
• Integrated Developm compilers, assemble:	nent Environment rs, emulators, logic a	(IDE) consists of analyzers.	f simulators with editors,	
IDE Components:				
<u>Editor:</u>				
• You can type your	assembly program-u	sing editor.		
• An editor is a progr	am which helps you	to construct your as	sembly language program in	
form of your progre	the assembler will the mis called as source	ansiate it correctly to	o machine language. This	
The assembly progra	am written using D(OS Editor is stored a	s . asm extension & The C	
Program written us	ng DOS Editor is sto	ored as .C extension	•	
Cross Assembler:	6			
An Cross Assemble	r is program that all	ows an Assembly pro	ogram written on one type of	
microcontroller to b	e used on another ty	rpe.		
<u>Simulator:</u>				
• Simulator Simulate Software.	s (Duplicates) the be	havior of Target Ha	dware (Microcontroller) in	
• Provides the detail	ed information of t	he status of RAM a	and ports (simulated) of the	
defined target syste	m and can execute e	ach instruction in Si	ngle step mode.	
Emulation:				
• An emulator in com	iputer sciences dupli	cates (provides an el	mulation of) the functions of	
to be) the first system	n.	that the second syste	in behaves like (and appears	
Logic Analyzer:				
• A logic analyzer is	an electronic instru	ment that captures a	and displays multiple signals	
from a digital system	n or digital circuit.	A logic analyzer m	ay convert the captured data	
into timing diagrams				
<u>RTOS:</u>				
• RTOS are used in a	system to execute a	ny task in defined	time limits. It has following	
tunctions.	langament			
1. Memory N 2 File Mana	gement			
2. I ne Iviana 2. Dort Mono	gement			

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		4. Process Management						
		5. I/O Management						
		<u>1 arget Process Evaluator:</u>						
		• Target Evaluation is the systematic process of gathering and analyzing data and other objective information on processing and subserving the quality makes and subserving the systematic process of gathering and analyzing data and other						
		objective information on processes and outcomes to determine the quality, value, and effectiveness of coding & performance improvement						
0.6			16-M					
C ¹⁰		Attempt any <u>FOUR</u> of the following:						
	a)	Draw structure of Interrupt and explain it.	4M					
	Ans	Interrupt Structure:	2Marks					
	:	IE register IP register High	for					
			Diagram					
		TF0 C C C C C C C C C C C C C C C C						
		TFI O O O O O O O O O O O O O O O O						
		TF2 (8052 only)						
		Individual						
		Global enable Accept interrupt						
		There are five interrupt sources on the 8051:						
		1. External 0 Interrupt						
		2. Timer 0 Interrupt						
		3. External 1 Interrupt						
		4. Limer Linterrupt 5. Serial Interrupt						
		All Interrupt are disabled after a system reset and are enabled individually by software. In the						
		event of two or more simultaneous interrupts or an interrupt occurring while another interrupt						
		is being serviced, there is both a polling sequence and a two level priority scheme to						
		schedule the interrupts. The polling sequence is fixed but the interrupt priority is						
		programmable.	Morka					
		As shown in the interrupt structure External 0 / External 1 interrupts can be level triggered or						
		Edge triggered.	ivi Evnlanat					
		IT0 / IT1 i.e. (ITx) in TCON are used to decide level triggering or edge	ion					
		triggering. If $ITx = 0$ then low level interrupt is used to trigger 8051 & if $ITx = 1$ then Falling	1011					
		edge will set IEx flag and interrupt is generated. IT0 & IT1 bits are available in TCON SFR.						
	b)	Draw the interfacing diagram of 3*3 keyboard matrix with 8051. Also explain logic to	4M					
	U)	read key.	-111T					

C - 2700 tified)

Ans	Vcc ç	2Marks					
:		for					
	R3 × R3	Diagram					
	Port 1 2° 2° 2°						
	$\begin{array}{c c} P1.0 \\ \hline \\ 5 \\ \hline \\ \end{array}$						
	8051 P1.1 P P P P						
	P1.2						
	R6						
	P2.0 P2.1 P2.2						
	8051 Port 2						
	Keyboard Logic to read keyboard:						
	1. Port P1 is used as an O/P port for microcontroller 8051 & Port 2 as an I/P port of	i microcontroller 8051 & Port 2 as an I/P port of that it gives low voltage when key is pressed. uning the port P2 by checking all columns for zero 2Marks					
	microcontroller 8051						
	3 See if any key is pressed by scanning the port P2 by checking all columns for zero						
	condition.	2Marks					
	4. If any key is pressed, to identify which key is pressed make one row low at a time.	for					
	5. Initiate a counter to hold the count so that each key is counted.	Explanat					
	6. Check port P2 for zero condition. If any zero number is there then start column scanning by following step 8	heck port P2 for zero condition. If any zero number is there then start column scanning ion					
	7. Otherwise make next row low in port P1 and repeat from step 6						
	Otherwise make next row low in port P1 and repeat from step 6 Fany key pressed is found, then content in accumulator is rotated right through the carry						
	until carry bit sets, while doing this increment the count in the counter till carry is found.						
	9. Move the content in the counter to display in data field or to memory location						
c)	10. To repeat the procedures go to step 2.	4M					
C)	List any four assembler uncerve and explain it.						
Ans	Following are Assembler directives	1Marks					
:	1. ORG	for Each					
	$\begin{array}{c} 2. \underline{EQU} \\ 3 DB \end{array}$	Assemble					
	4. DW	r					
	5. <u>END</u>	Directive					
	(1) <u>ORG (Originate):</u>						
	From the Program						
	<u>Address</u> Hey						
	Org 0400h becomes 0400 79						
	Mov r2. $\#00h$ 0401 00						
	The ORG pseudo lets you put code and data anywhere in program memory you wish.						
	Normally the program starts at 0000h using an org 0000h.						
	(2) <u>EOU (Equate):</u>						
	Label equxxxxEquate the label name to the number xxxx						

	Example progra	ım							
			Address	Hex	Σ.				
	Org 0000h	becomes	0000	74					
	Fredequ 12h		0001	12					
	Mov a, #fred								
	EQU turns numbers into names; it makes the program much more readable because the name								
	chosen for the label can have some meaning in the program. whereas the number will not.								
	(3) DB(Define H	3vte)	0 1 0						
	db xx Define a byte: Place the 8 bit number xx next in memory.								
	Example program								
			Address	Hex					
	Org 0100h	becomes	0100	34					
	db 34h		0101	56					
	db 56h		0101	00					
	DB vy takes the number vy (from 0 to 255) and converts it to hav in the next memory location								
	DB AX takes the number AX (non 0 to 255) and converts it to nex in the next memory location.								
	(4) DW (Define word):								
	(4) <u>DW (Define word)</u> : dwyyyy Define aword: place the 16bit number yyyy in memory								
	Fyample program	m			emory.				
		111	66 A	Moda	Uov				
	org Oshadh	bacomac	Auu	1055	12				
	org Oabcun	becomes	abcu		12				
	dW 1254n		abce		34				
	 DW is a 16 bit version of db. (5) End: The End: Tells the assembler to stop assembling 								
<u>-1)</u>									
a)	Draw the struct	ure of internal RAM	01 8051.			4111			
Ans				Bit Addresses		4 Marks			
:	Bank 0	70			Byte Addresses	for			
-	ſ	08	00 01	02 03 04 05	06 07 20	Correct			
	Bank 1	0F	08 09	OA OB OC OD	DE OF 21	Diagram			
	Bank 2	10	10 11	12 13 14 15	16 17 22	Diagram			
		17	18 19	1A 1B 1C 1D	1E 1F 23				
	Bank 3	16 1F	20 21	22 23 24 25 2	26 27 24				
	(20		1					
	Bit 🗸								
	Addressable	2F							
	C .	20							
	Scratch	30							
	Scratch Pad Area		70 71	72 73 74 75	76 77 2E				
	Scratch Pad Area	25	70 71 78 79	72 73 74 75 7A 7B 7C 7D	76 77 2E 7E 7F 2F				
	Scratch Pad Area	7F	70 71 78 79	72 73 74 75 7A 7B 7C 7D	76 77 2E 7E 7F 2F				



MAHARASHTI

