

17627

**11920**

**3 Hours / 100 Marks**

Seat No.

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- Instructions :**
- (1) All Questions are *compulsory*.
  - (2) Illustrate your answers with neat sketches wherever necessary.
  - (3) Figures to the right indicate full marks.
  - (4) Mobile Phone, Pager and any other Electronic Communication devices are not permissible in Examination Hall.

- |   | <b>Marks</b> |
|---|--------------|
| <b>1. Solve any FIVE of the following :</b>                               | <b>20</b>    |
| (a) State any eight features of 80386.                                    |              |
| (b) Describe Hardware & Software interrupts.                              |              |
| (c) State any eight salient features of Pentium Processor.                |              |
| (d) State advantages of RISC Processor. (any four)                        |              |
| (e) What are data independence issues in RISC ?                           |              |
| (f) Distinguish between .com & .exe programs. (any 4 points)              |              |
| (g) What is self-test ?   |              |
| <b>2. Attempt any TWO of the following :</b>                              | <b>16</b>    |
| (a) Draw and explain Pentium system architecture.                         |              |
| (b) Write an ALP for function 02H & function 09h of INT 21H with example. |              |
| (c) Draw & explain stages of pipelining in RISC Processor.                |              |

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P.T.O.

- 3. Attempt any FOUR of the following : 16**
- (a) Explain the register organization of 80386 microprocessor with neat diagram.
  - (b) List any eight features of SUN ultra SPARC.
  - (c) With neat sketch, explain branch prediction of Pentium.
  - (d) Draw & explain DOS-BIOS interface.
  - (e) Draw control flags of 80386.
- 4. Attempt any FOUR of the following : 16**
- (a) Draw Register set of Pentium processor.
  - (b) Explain floating point exceptions in Pentium.
  - (c) Explain Hybrid Architecture of RISC & CISC.
  - (d) Explain INTO & IRET instruction.
  - (e) Describe superscalar architecture of Pentium Processor with neat diagram.
- 5. Attempt any FOUR of the following : 16**
- (a) Explain the concept of segment descriptor cache register of 80386.
  - (b) Draw & explain Intel MMX architecture of registers.
  - (c) Explain structure of MS-DOS with neat diagram.
  - (d) Compare between 80386 and Pentium. (any four points)
  - (e) Describe code/data segment descriptor of 80386.
- 6. Attempt any TWO of the following : 16**
- (a) Write difference between Real Mode and PVAM mode. (Any eight points)
  - (b) Describe the eight stage pipelining mechanism in floating point unit of Pentium Processor with neat diagram.
  - (c) What do you mean by TLB ? How does it help in address calculation procedure ?
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