Important Instructions to examiners:

1) The answers should be examined by key words and not as word-to-word as given in the model answer scheme.
2) The model answer and the answer written by candidate may vary but the examiner may try to assess the understanding level of the candidate.
3) The language errors such as grammatical, spelling errors should not be given more Importance (Not applicable for subject English and Communication Skills.
4) While assessing figures, examiner may give credit for principal components indicated in the Figure. The figures drawn by candidate and model answer may vary. The examiner may give credit for any Equivalent figure drawn.
5) Credits may be given step wise for numerical problems. In some cases, the assumed constant Values may vary and there may be some difference in the candidate's answers and model answer.
6) In case of some questions credit may be given by judgment on part of examiner of relevant answer based on candidate's understanding.
7) For programming language papers, credit may be given to any other program based on equivalent concept.

1. A) Attempt any five: **20M**

a) Convert the following decimal numbers into excess — 3 code.

i) $(7)_{10}$ ii)$(45)_{10}$ iii) $(232.8)_{10}$

Ans: **04M**

a) Convert the following decimal Number into excess-3 code

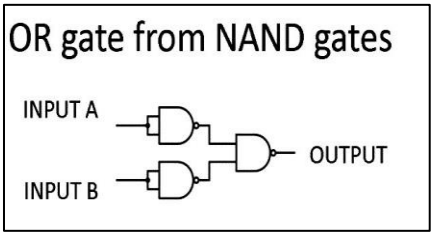
i) $(7)_{10} = 0111 + 0011 = (1010)_{E3C}$

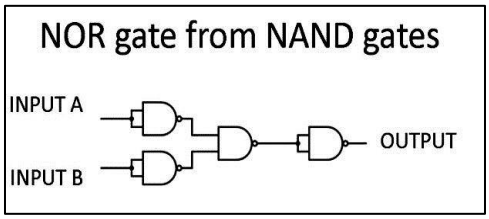
ii) $(45)_{10} = 0100\ 0101 + 0011\ 0011 = (0111\ 1000)_{E3C}$

iii) $(232.8)_{10} = 0010\ 0011\ 0010.1000 + 0011\ 0011\ 0011.0011 = (0101\ 0110\ 0101.1011)_{E3C}$

b) Draw the logical diagram of OR gate and NOR gate using NAND gate only.

Ans: **02M for each diagram**





c) Convert the following expression in standard SOP form. Y =AB +AC + BC.

Ans: **04M**

$$Y = AB + AC + BC$$

$$Y = AB(C + \bar{C}) + AC(B + \bar{B}) + (A + \bar{A})BC$$

$$= ABC + AB\bar{C} + ABC + A\bar{B}C + ABC + \bar{A}BC$$

$$= ABC + AB\bar{C} + A\bar{B}C + \bar{A}BC .$$

d) Compare between combinational and sequential logic circuits. (Any 04 points).

Ans: **(Any four points)** **01M each**

PARAMETERS	COMBINATIONAL CIRCUIT	SEQUENTIAL CIRCUIT
Definition	The output at any instant of time depends upon the input present at that instant of time.	The output at any instance of time depends upon the present input as well as past input and output.
Need of Memory	No memory element required in the ckt	Memory element required to stored bit
Need of clock	Clock input not necessary	Clock input necessary
Examples	E.g. Adders, Subtractors ,Code converters, comparators etc.	E.g. Flip flop, Shift registers, counters etc,
Applications	Used to simplify Boolean expressions, k-map , Truth table	Used in counters & registers

e) State any four features of PCF 8591.

Ans:

FEATURES (Any four):- **01M each**

1. Single power supply
2. Operating supply voltage 2.5 V to 6 V
3. Low standby current
4. Serial input/output via I2C-bus
5. Address by 3 hardware address pins
6. Sampling rate given by I2C-bus speed
7. 4 analog inputs programmable as single-ended or
8. differential inputs
9. Auto-incremented channel selection
10. Analog voltage range from VSS to VDD
11. On-chip track and hold circuit
12. 8-bit successive approximation A/D conversion
13. Multiplying DAC with one analog output

f) State different types of ROM and explain anyone in detail.

Ans: **Types 1M, Explanation 3M**

There are five basic ROM types:

1. ROM - Read Only Memory.
2. PROM - Programmable Read Only Memory.
3. EPROM - Erasable Programmable Read Only Memory.
4. EEPROM - Electrically Erasable Programmable Read Only Memory.
5. Flash EEPROM memory.

Explanation :- (any one)

Flash Memory:-

1. Flash memory is non-volatile RAM memory that can be electrically erased and reprogrammed.
2. Flash memory can be written to in block size rather than bytes; it is easier to update it.
3. Due to this, the flash memories are faster than EEPROMS which erase and write new data of byte level.
4. This type of memory has been named as ‘flash memory’ because a large block of memory could be erased at one time, i.e. in a single action or ‘flash’.
5. Important features are high speed, low operating voltage low power consumption.
6. Typically applications areas are digital camera`s embedded controllers, cellular phones etc.

OR

Programmable Read Only Memories (PROM):-

PROM is electrically programmable i.e. the data pattern is defined after final packaging rather than when the device is fabricated. The programming is done with an equipment referred to as PROM programmer. The PROM are one time programmable. Once programmed, the information stored is permanent.

OR

Erasable Programmable Read Only Memories (EPROM):-

In these memories, data can be written in any number of times i.e. they are reprogrammable . Reprogrammable ROMs are possible only in MOS technology. For erasing the contents of the memory, one of the following two methods are employed:

a) Exposing the chip to ultraviolet radiation for about 30minutes (UVEPROM)
b) Erasing electrically by applying voltage of proper polarity & amplitude. Electricity erasable Prom is also referred to as E^2PROM or EEPROM or EAROM (Electrically alterable ROM)

In this data is stored in the form of charge.

g) State the number of Flip Flops required to construct the following modulus of counter.

i) 7 ii) 85 iii) 98 iv) 11

Ans: **4M**

g) No. of F/F required

i) 7 – 3 F/Fs.
ii) 85 – 7 F/Fs
iii) 98 – 7 F/Fs.
iv) 11 – 4 F/Fs.

Q.2. Attempt any FOUR: **16M**

a) Perform binary subtraction using 2's complement method $(11001)_2 - (1010)_2$

Ans:

```
  1 1 0 0 1
- 0 1 0 1 0
-----------
```

2's Compliment

```
0 1 0 1 0
1st compliment
1 0 1 0 1
+       1
---------
1 0 1 1 0
```

2M

```
  1 1 0 0 1
+ 1 0 1 1 0
-----------
1 0 1 1 1 1
```

Discard the carry

Final Answer is $(0\ 1\ 1\ 1\ 1)_2$ **2M**

b) State De Morgan's theorem and prove by Truth-table method for two variables.

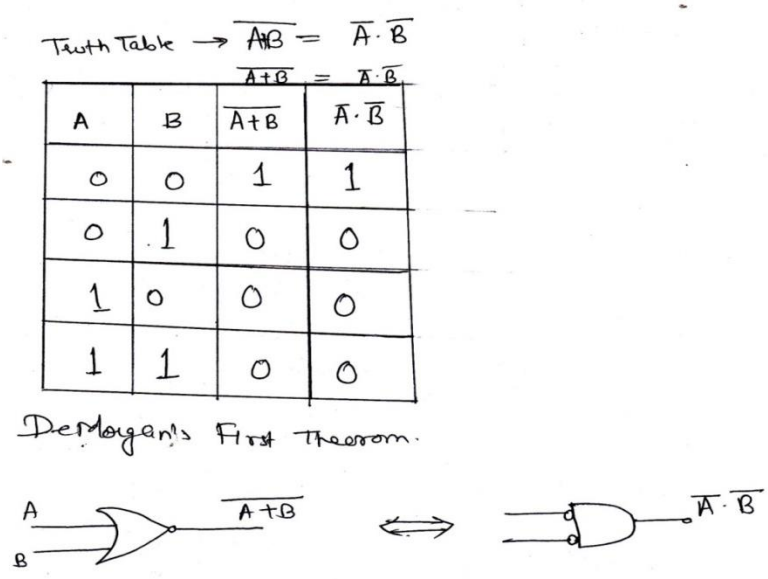
Ans: **02M to each Theorem**

a) De Morgan's First Theorem:

$$\overline{A+B} = \overline{A} \cdot \overline{B}$$

It states that the complement of sum equals the product of complements.

Verification of De Morgan's Theorem first law



The value of $\overline{A+B}$ in the column 3 is the same as that of $\overline{A}\ \overline{B}$ in the column 4 for each of the possible combinations of the variables A & B.

b) De Morgan's Second Theorem:

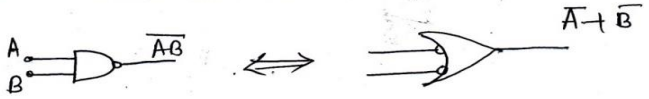
$$\overline{A.B} = \overline{A} + \overline{B}$$

It states that the complement of product equals the sum of the complements

Verification of De Morgan's Theorem second law

Truth Table for $\overline{A \cdot B} = \overline{A} + \overline{B}$

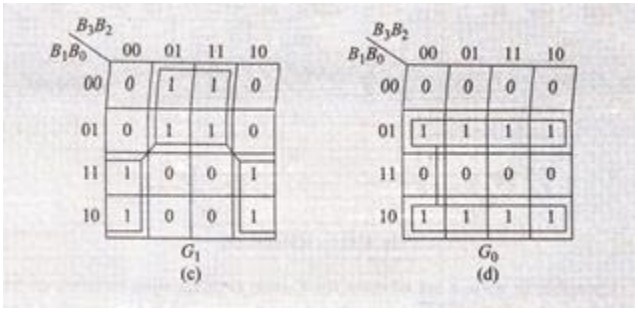
A	B	$\overline{A \cdot B}$	$\overline{A}+\overline{B}$
0	0	1	1
0	1	1	1
1	0	1	1
1	1	0	0

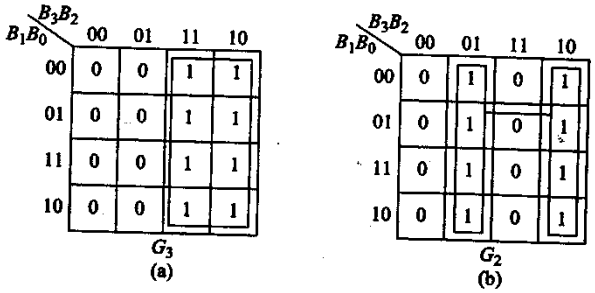


The value of $\overline{A \cdot B}$ in the column 3 is the same as that of $\overline{A+B}$ in the column 4 for each possible combinations of the variables A & B.

C) Give the expression of Grey code equivalent of 4-bit binary using K-map.

Ans: **K-map 02M, diagram 01M, truth table 01M**



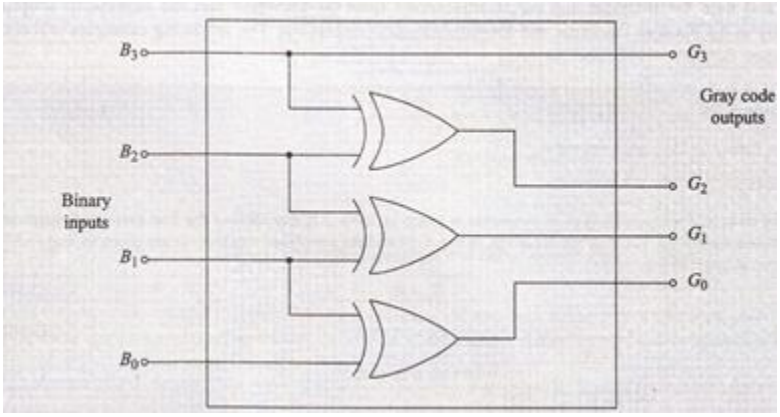


$$G_3 = B_3$$

$$G_2 = B_2 \oplus B_3$$

$$G_1 = B_1 \oplus B_2$$

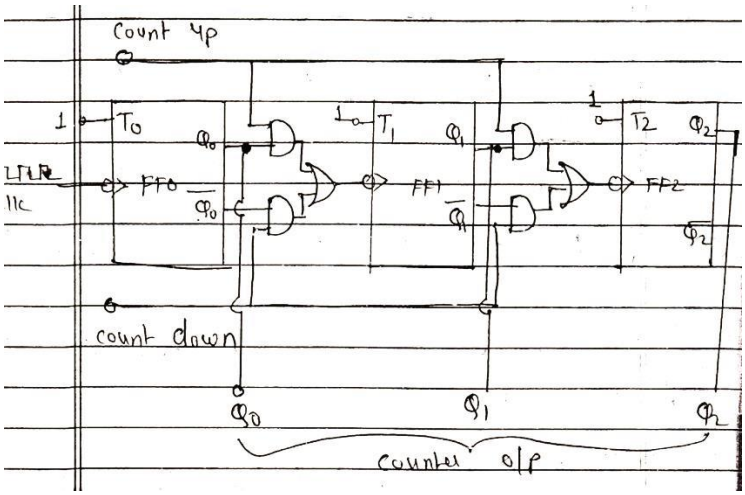
$$G_0 = B_0 \oplus B_1$$



Binary Input				Gray code output			
B_3	B_2	B_1	B_0	G_3	G_2	G_1	G_0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

d) Draw the circuit diagram of 3-bit asynchronous up/down counter using T-FF.

Ans: **04M**



e) Describe any four specifications of DAC.

Ans: (Any four) 01M each

The characteristics of a DAC converter which are generally specified by the manufactures are

1) Resolution
2) Accuracy
3) Setting time or DAC speed
4) Gain
5) Temperature sensitivity
6) Linearity
7) Monotonicity

1) **Resolution**:-

It is defined as the smallest possible change in the output voltage as a fraction or percentage of the full scale output range it can be produced by a single step change in digital input.

2) **Accuracy**:-

The accuracy of DAC is a measure of difference between the actual output as a percentage of full scale or maximum output voltage.

3) **Setting time or DAC speed**:-

The operating speed of a DAC is usually specified by giving its setting time which is the time required for the DAC output to go from zero to full scale as the binary input is changed from 0 s to all 1s. Actually the setting time is measured as the time for the DAC output to settle within ±½ step size of its final value.

4) **Gain:-**

It is defined as the ratio of the output voltage at DAC to the analog equivalent of digital input.

5) **Temp sensitivity:**

The parameters of active and passive devices varies with temp. These changes affects the analog output voltage of DACs. It is specified as ±pp m/^{o}c.

6) **Linearity:** -

In DAC converters, equal increments in the numerical significance of the digital input should result in equal increment in the analog output voltage. In a actual circuit, the input output relationship is not linear. This is due to the error in the resistor values and voltage across the switches. The linearity of the converter is a measure of the precision with which the linear input output relationship is satisfied.

7) **Monotonicity:-**

It is defined as the quality of DAC having no differential linearity problem. Thus monotonicity implies ±½ LSB accuracy.

f) Compare volatile and non -volatile memories (any 4 pts.)

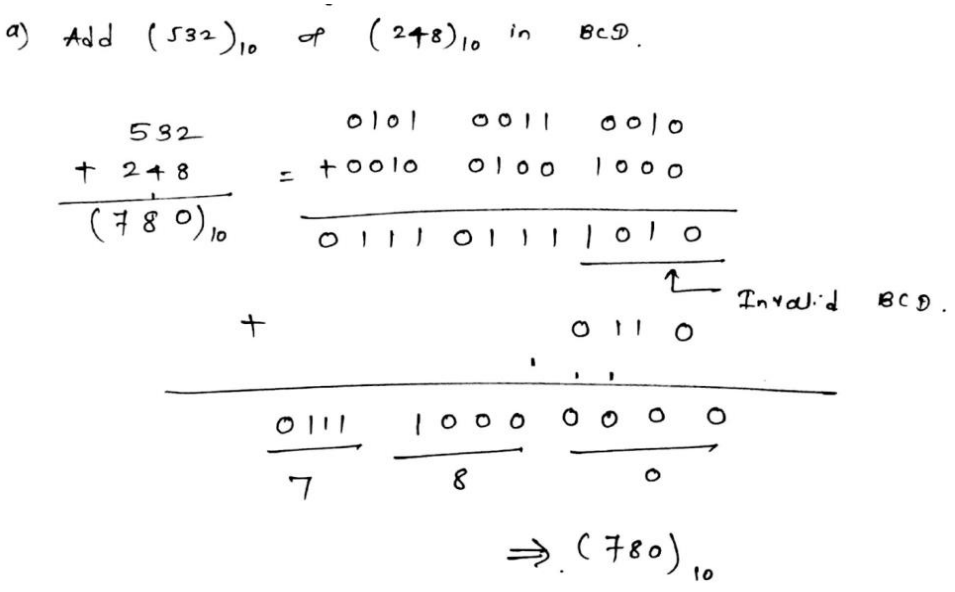
Ans: (Any four) **01M each**

Sr No.	Parameter	Volatile	Non-volatile
1.	**Definition**	Information stored is lost if power is turned off	Information stored is not lost even if power goes off
2.	**Classification**	All RAMs	ROMs, EPROMs
3.	**Effect of power**	Stored information is retained only as long as power is ON	No effect of power on stored information
4.	**Application**	For temporary storage of data.	For permanent storage of data.
5.	**Devices used**	Volatile memory devices are mainly solid state devices	Nonvolatile memory can be sold state, magnetic or optical
6.	**Speed**	Volatile memory is very fast in data processing	Nonvolatile memory is slow in data processing as compared to volatile.

3. Attempt any four : **16M**

a) Add $(532)_{10}$ and $(248)_{10}$ in BCD.

Ans: **4M**



b) Compare TTL and CMOS logic families on the basis of size, power, cost and speed.

Ans: **01M each**

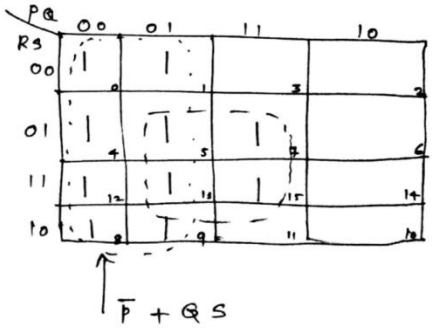
PARAMETERS	TTL	CMOS
Size	Large	Small
Power	10mw	10nw
Cost	More expensive	Less expensive
Speed	Faster	Slower

c) Minimize following expression using K-map f (P, Q, R, S) = ∑m (0, 1, 4, 5, 7, 8, 9,12,13,15).

Ans: **04M**

c) minimize using k-map

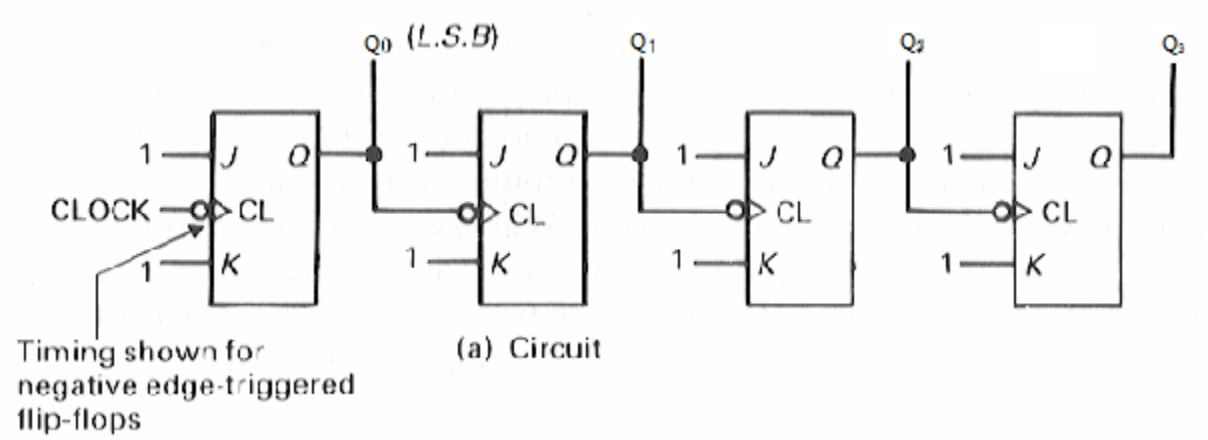
$f(P, Q, R, S) = \sum m(0, 1, 4, 5, 7, 8, 9, 12, 13, 15)$



d) Describe the working of 4-bit ripple counter with logic diagram and waveforms.

Ans: **Diagram 1 M,Explanation 1M,Waveform 1M,Truth Table 1M**

NOTE :* - *Explanation in short can be considered,Marks can be given on basis of Truth table,waveform



Working :-

(1) Initaially clock = 0
Therefore all the flip flop be in reset condition
Therefore $Q_3Q_2Q_1 Q_0 = 0000$

(2) On the 1st -ve going clock edge

- As soon as the 1st falling edge of the clock is given to FF 0, it will toggle as $T_0 = 1$

Hence $Q_0 = 1$

- Q_0 is connected to clock input of FF1. Since Q_0 has changed from 0 to 1, it is treated as the +ve clock edge by FF1.

- Therefore no change in Q_1 because FF1 is a –ve edge triggered.
- After 1st clock pulse the counter outputs are $Q_3Q_2Q_1\ Q_0 = 0001$

(3) At the 2nd falling edge of the clock

- On the arrival of 2nd falling edge, FF0 toggles again, to make $Q_0 = 0$.
- This change in Q_A (from 1 to 0) acts as –ve clock edge for $Q_1 = 1$
- Hence after 2nd clock pulse the counter output are $Q_3Q_2Q_1\ Q_0 = 0010$

(4) At the 3rd falling edge of clock

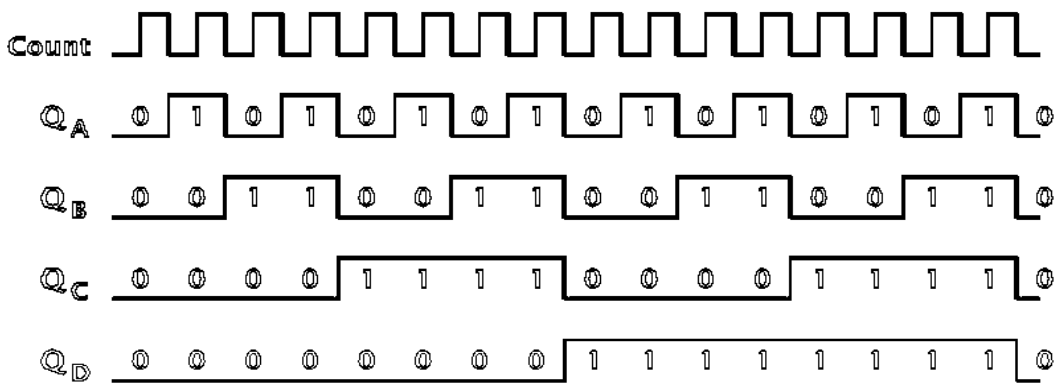
- On arrival of 3rd falling edge FF0 toggles again & Q_0 becomes 1 from 0
- Since this is +ve going change [0 to 1] FF 1 does not respond to it & remains inactive. So Q_1 does not change. Therefore $Q_3Q_2Q_1\ Q_0 = 0011$ and so on till the 16th clock pulse and then the counter reached the final count i.e. $Q_3Q_2Q_1\ Q_0 = 1111$.After 16th clock pulse the operation of counter repeats.

Truth table:-

Input clock pulse	**Q_3**	**Q_2**	**Q_1**	**Q_0**	**Decimal equivalent count**
	**0**	**0**	**0**	**0**	**0**
	**0**	**0**	**0**	**1**	**1**
	**0**	**0**	**1**	**0**	**2**
	**0**	**0**	**1**	**1**	**3**
	**0**	**1**	**0**	**0**	**4**
	**0**	**1**	**0**	**1**	**5**
	**0**	**1**	**1**	**0**	**6**
	**0**	**1**	**1**	**1**	**7**
	**1**	**0**	**0**	**0**	**8**
	**1**	**0**	**0**	**1**	**9**
	**1**	**0**	**1**	**0**	**10**
	**1**	**0**	**1**	**1**	**11**
	**1**	**1**	**0**	**0**	**12**

↓	1	1	0	1	13
↓	1	1	1	0	14
↓	1	1	1	1	15
↓	0	0	0	0	0 (count repeats)

Waveform:-



e) State advantages and disadvantages of single slope ADC.

Ans:

Advantages of single slope ADC: **2M**

- It is very simple in construction.
- It is easy to design
- It is less expensive.
- It is faster than dual slope ADC.

Disadvantages of single slope ADC: **2M**

- It is comparatively very slow.
- Conversion time does not remain constant.
- It needs longer conversion time.

f) Describe the working of Flash-memory.

Ans:

Flash Memory: **4M**

1. Flash memory is non-volatile RAM memory that can be electrically erased and reprogrammed.
2. Flash memory can be written to in block size rather than bytes; it is easier to update it.
3. Due to this, the flash memories are faster than EEPROMS which erase and write new data of byte level.

4. This type of memory has been named as 'flash memory' because a large block of memory could be erased at one time, i.e. in a single action or 'flash'.
5. Important features are high speed, low operating voltage low power consumption.
6. Typically applications areas are digital camera`s embedded controllers, cellular phones etc.

Q.4 Attempt any FOUR: **16M**

a) State the rules for BCD addition.

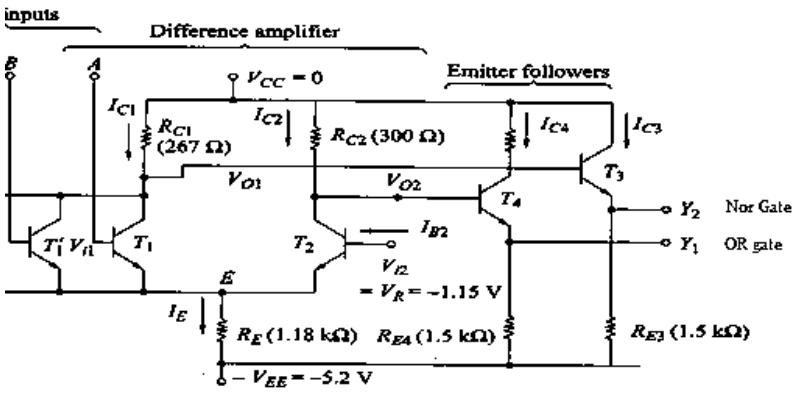
Ans: **04M**

BCD Addition

Case 1	Case 2	Case 3
Sum ≤ 9 Carry = 0	Sum ≤ 9 Carry = 1	Sum > 9 (Invalid BCD) Carry = 0
↓	↓	↓
Answer is correct	Add 6 to the sum to get correct answer	Add 6 to the sum to get correct answer
For example decimal BCD 2 0010 +6 +0110 8 0 1000 ↑ carry valid BCD	9 1001 +8 +1000 17 (1) 0001 ↑ carry ∴ Add 6 to the sum 1 0001 + 0110 1 0111 ↓ ↓ ans. (1 7)	7 0111 +6 +0110 13 1101 ↑ invalid BCD ∴ add 6 1101 + 0110 1 0011 ans (1 3)

b) Draw two input OR gate, using ECL logic family (only diagram).

Ans: **04M**



c) Realize full subtractor using K-map.

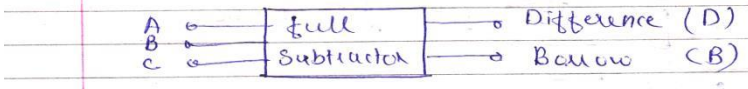
Ans: **01M truth table, 011/2M K map, 011/2M logical diagram**

It has 3 inputs, A_n(minued),B_n (subtrahend) & C_{n-1} (borrows from previous stage) & two outputs (difference & borrow).

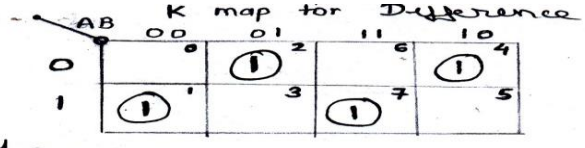
Truth table

Input			Output	
A_n	B_n	C_{n-1}	Difference	Borrow
A	B	C	D	B
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Logic Diagram

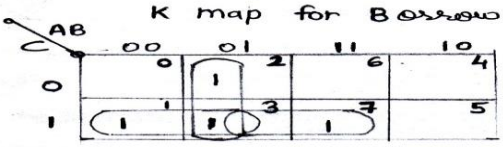


K map for Difference



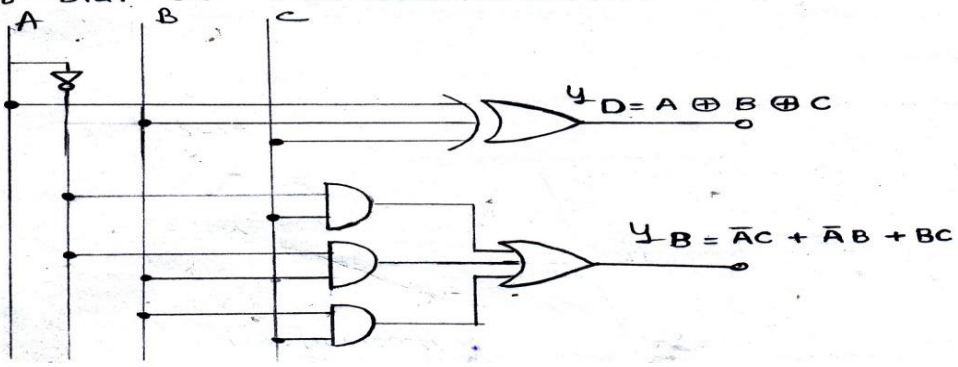
$Y_D = A \oplus B \oplus C$

K map for Borrow



$Y_B = \bar{A}C + \bar{A}B + BC$

ckt Dia. of Full Substractor →

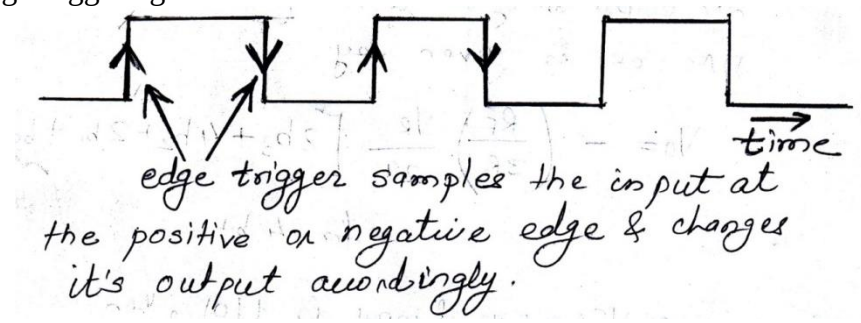


d) Describe positive and negative edge triggering methods of clock with their logical symbol.

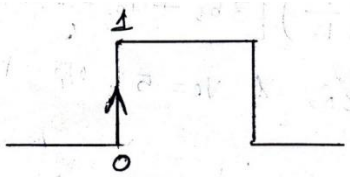
Ans: **02M each triggering**

The edge at which the transitions of clock pulse occurs from low to high is called rising/leading edge of clock pulse .Similarly the edge at which the transition of clock pulse occurs from high to low is called falling edge or trailing edge of clock pulse.

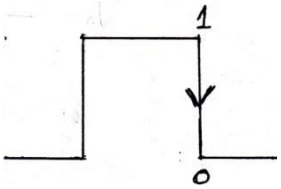
When the flip-flop is triggered by the leading or falling edge of the clock pulse to change its output state, it is called edge triggering.



- **+ ve edge triggering:**
  Changes from 0 to 1 if FF responds to rising edge of the c/ k pulse or to +ve voltage spikes, it is known as 'positive edge triggered FF.



- **- ve edge triggering:**
  Changes from 1 to 0. If FF responds to falling edge of the c/k pulse or to –ve voltage spikes, it is known as –ve edge triggered flip flop.



e) Calculate the analog output of 4-bit DAC if the digital input is 1101.Assume VFS=5V.

Ans: **04M**

The output analog voltage V_o by 4-bit R-2R ladder N/w DAC ckt is given by.

$$V_o = -\left(\frac{R_F}{3R}\right)\frac{V_R}{24}\left[8b_3 + 4b_2 + 2b_1 + b_0\right]$$

--- for 4-bit.

When $V_{FS} = 5V$, & input is 1101, then

$$V_o = -\frac{R_F}{3R}\left(\frac{V_R}{16}\right)\left[3b_3 + 2b_2 + 2b_1 + b_0\right]$$

if $R_F = 3R$, & $V_R = 5$, i/p = 1101,

$$V_o = -\frac{5}{16}\left[8(1) + 4(1) + 2(0) + 1\right]$$

$$V_o = -5/16\left[8+4+1\right]$$

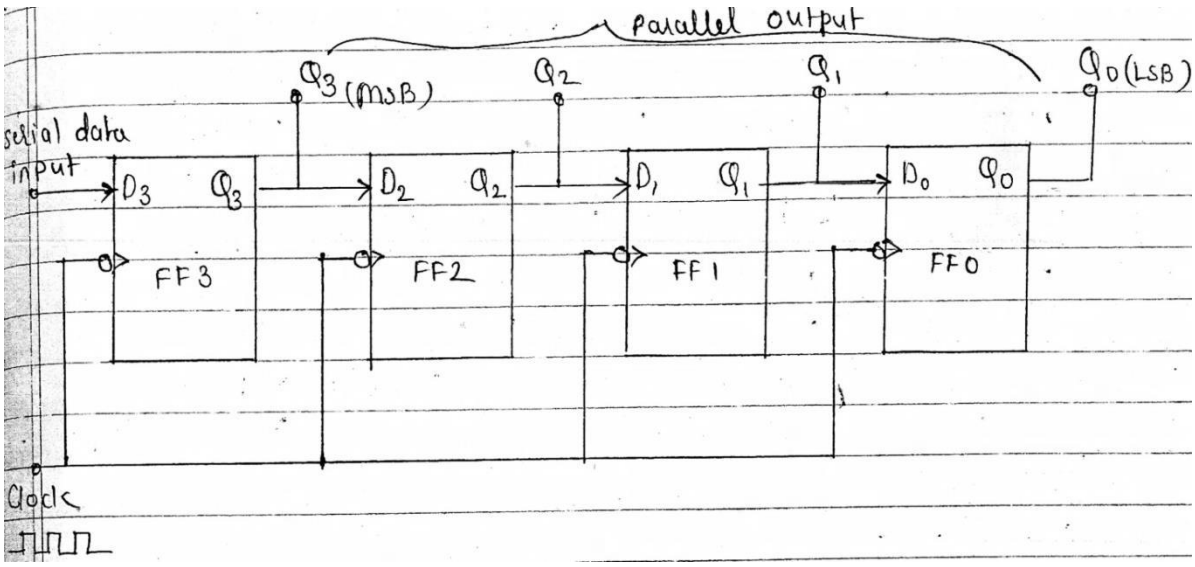
$$V_o = -4.0625\ V$$

The negative sign indicates output is taken from non- inverting mode of amplifier. Which can be ignored.

f) Draw the logic diagram of 4-bit SIPO shift register and explain its working principle.

Ans: **02M diagram & 02M for working**

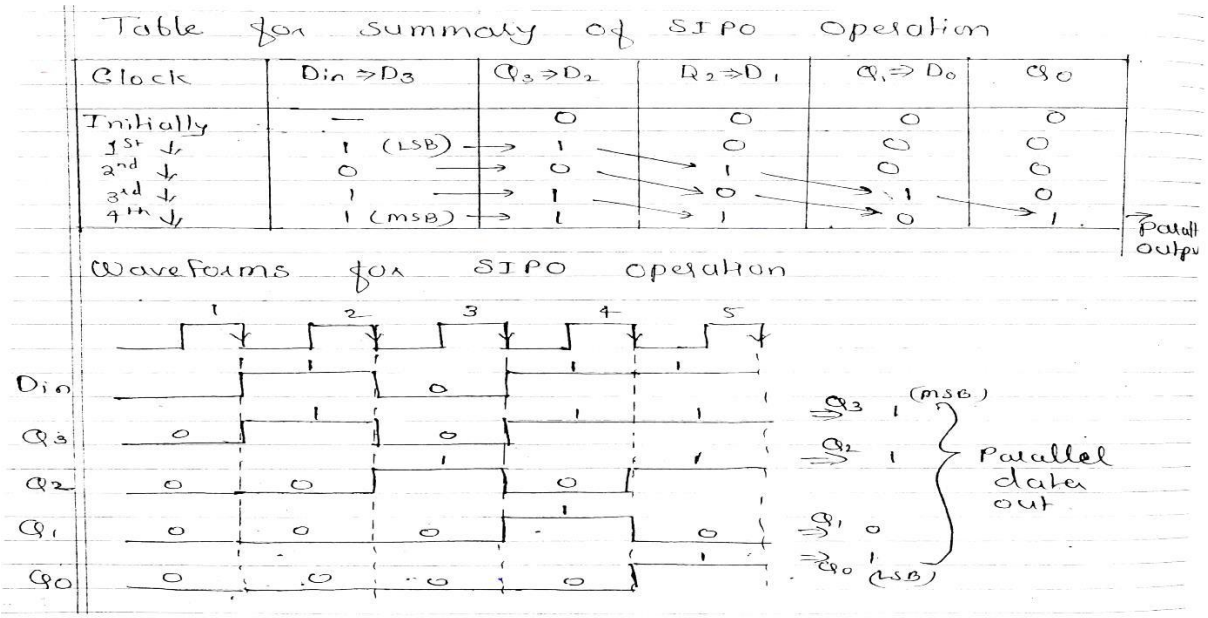
NOTE :Truth table& Waveform can be considered in working



Explanation:-

- The serial input parallel output shift register is shown above (SIPO).
- It accepts the input data serially i.e. one bit at a time and outputs the stored data in parallel form.
- At the end of each clock pulse (-ve edge) a first data bit of higher significant bit(as LSB is entered first) enters into the D_i i/p of FF_1 and Q output of every FF gets shifted to the next FF on right side.
- Thus once the data bits are stored, each bit appears on its respective output line & all bits are available simultaneously at Q_3 Q_2 Q_1 Q_0 rather than an a bit by bit basis with the serial output.

D in=1101

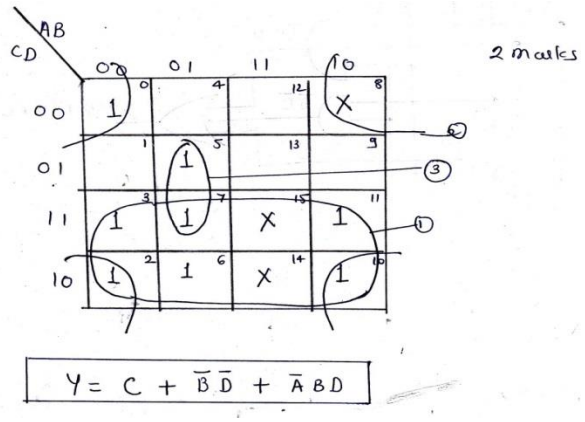


Q5 Attempt any four: **16M**

a) Realize the following expression using K-map.

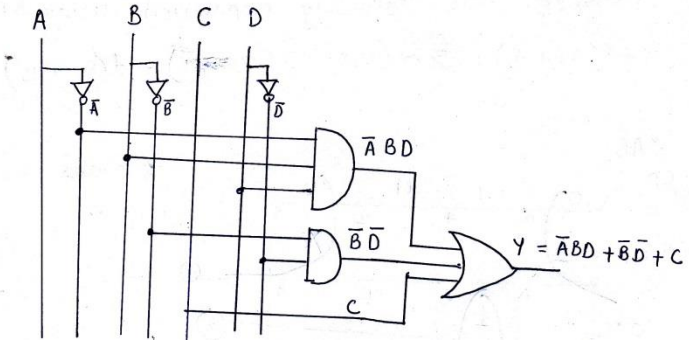
Y = f(A, B, C, D) = ∑m (O, 2, 3, 5, 6, 7, 10, 11) + d (8, 14, 15) and implement it

Ans:- **K Map 2M ,Design 2M**



Circuit diagram —— 2 marks.

$Y = C + \bar{B}\bar{D} + \bar{A}BD$



b) Simplify the following expression using Boolean laws

$Y = (A + B)(A + C)$

$Y = ABC + A\bar{B}C + AB\bar{C}$

Ans:-

$Y = (A+B)(A+C)$ 2 marks

$Y = AA + AC + AB + BC$

$Y = A + AC + AB + BC$ $\because AA = A$

$Y = A(1 + C + B) + BC$

$Y = A + BC$ $\because (1+A) = 1$ & $A \cdot 1 = A$

$Y = ABC + A\bar{B}C + AB\bar{C}$ 2 marks

$Y = AC(B+\bar{B}) + AB\bar{C}$

$Y = AC + AB\bar{C}$

$Y = A(C + \bar{C}B)$

$\boxed{Y = A(B+C)}$ $\because A + \bar{A}B = A + B$

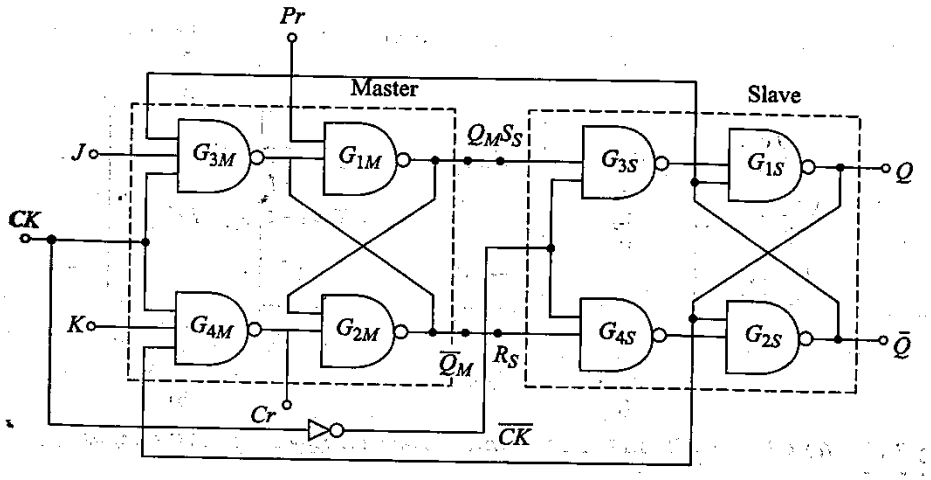
OR

(A+B)(A+C)
AA+AC+BA+BC
=A+AC+AB+BC since, A+A=A and BA=AB
=A(1+C)+AB+BC
=A+AB+BC since1+c=1
=A(1+B)+BC
=A+BC since1+B=1

c) Draw the circuit of master slave JK FF using NAND gate and list its advantages

Ans:- **03M circuit diagram, 01M advantage**

Diagram:-



Advantage:-

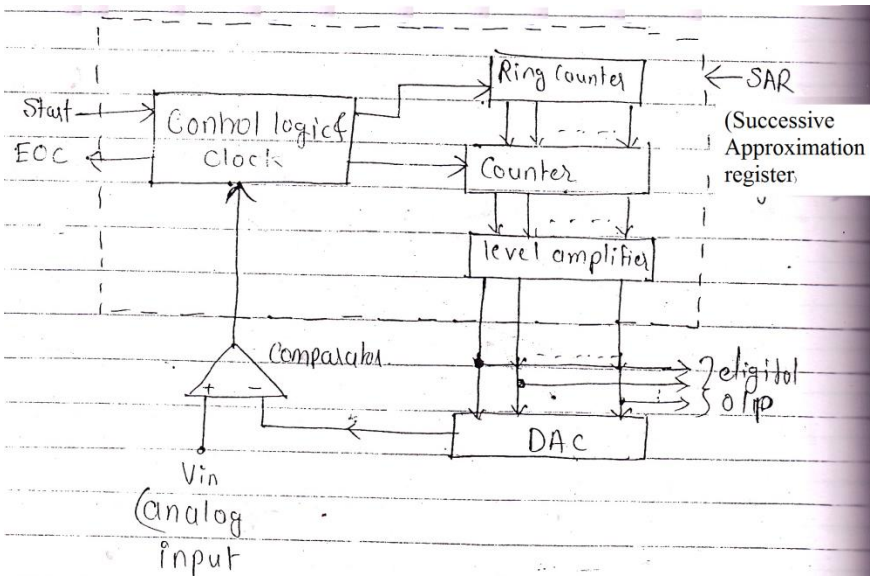
1) Race around condition is avoided
2) Triggering circuit is simple and easy to design.

c) Draw and explain the block diagram of successive approximation method ADC.

Ans:- **02M diagram, 02M explanation**

NOTE:- Any other relevant diagram & explanation can be considered

Diagram:-



Explanation:-

- The Counter is first reset to all 0s and then MSB is set. Then the SAR waits for a signal from comparator indicating whether the DAC output is greater or less than the analog input voltage. If the comparator output is high, then the DAC output is less than V_{in} & SAR will keep the MSB set. If the comparator output is low, then the DAC output is greater than V_{in} & SAR will reset the MSB. SAR will set the next MSB on the next clock pulse. It will keep or reset this bit depending on the output from the comparator.. This process is repeated down to the LSB & at this time the desired number is in the counter. Since the conversion involves operating on a one bit or one FF at a time ,beginning with the MSB , the ring counter is used to select MSB or FF. the SAR keeps a bit if the D/A output is less than V_{in} & reset a bit if the D/A output is less than V_{in}. Only one clock pulse is needed for each such bit.
- Thus this method is the process of approximating the analog voltage by trying a 1- bit at a time beginning with the MSB. This conversion also called as serial conversion.

d) Convert the given binary number into decimal, hexadecimal, octal and grey code $(10111101)_2$

Ans:- **01M each**

① decimal → 1 mark

1	0	1	1	1	1	0	1
2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

$= 1\times2^7 + 1\times2^5 + 1\times2^4 + 1\times2^3 + 1\times2^2 + 1\times2^0$

$= 128 + 32 + 16 + 8 + 4 + 1$

$(10111101)_2 = (189)_{10}$

② Hexadecimal → 1 mark

$= \underbrace{1011}\underbrace{1101}$

$= B \quad D$

$(10111101)_2 = (BD)_H$

③ Octal → 1 mark

$= \underbrace{010}\underbrace{111}\underbrace{101}$

$2 \quad 7 \quad 5$

$(10111101)_2 = (275)_8$

④ Grey →

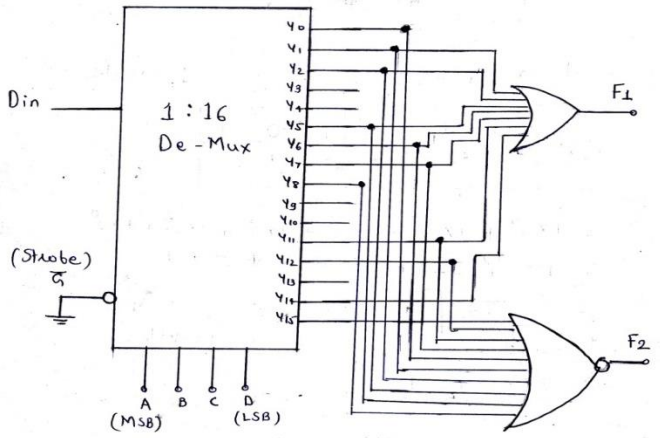
1	0	1	1	1	1	0	1
↓	⊕	⊕	⊕	⊕	⊕	⊕	⊕
1	1	1	0	0	0	1	1

$\therefore (10111101)_2 = (11100011)_G$

e) Implement the following function using de-multiplexer.
$F_1 = \sum m(1,2,5,6,7,11,14)$
$F_2 = \pi M(0,1,2,5,6,7,8,11,12,15)$

Ans:- **02M each**

$F_1 = \Sigma m\,(1,2,5,6,7,11,14)$ 2 marks
$F_2 = \pi M\,(0,1,2,5,6,7,8,11,12,15)$ 2 marks

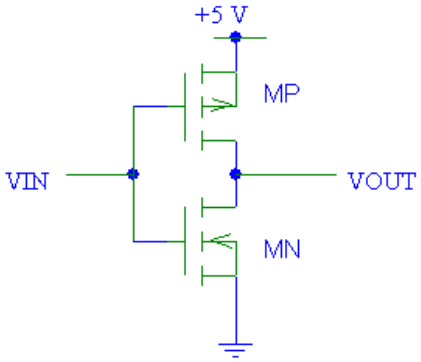


Q6 Attempt any four: **16M**

a) Describe CMOS inverter with diagram.

Ans:- **02M diagram, 02M explanation**

Diagram:-

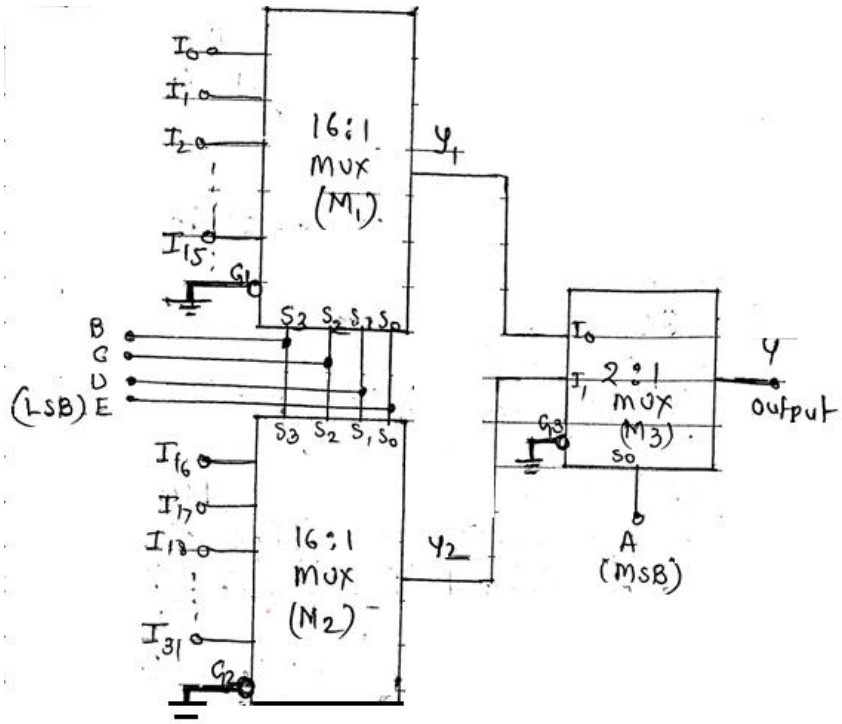


Description:-

The basic CMOS logic circuit is an inverter shown in fig. For this circuit the logic levels are 0V (logic 0) and V_{cc} (logic 1). When $V_1 = V_{cc}$, T_1 turns ON and T_2 turns OFF. Therefore $V_0 \approx 0V$, and since the transistors are connected in series the current I_D is very small. On the other hand, when $V_1 = 0V$, T_1 turns OFF and T_2 turns ON giving an output voltage $V_0 \approx V_{cc}$ and I_D is again very small. In either logic state, T_1 or T_2 is OFF and the quiescent power dissipation which is the product of the OFF leakage current and V_{cc} is very low. More complex functions can be realized by combinations of inverters.

b) Design 32: 1 multiplexer using 16: 1 multiplexer and one 2 : 1 multiplexer.

Ans:- **04M**



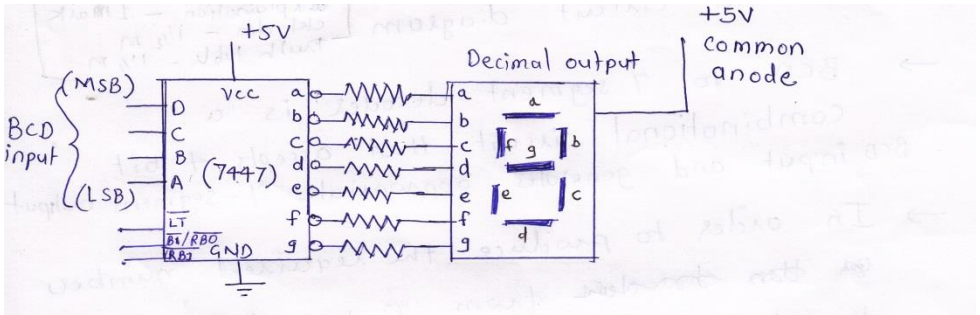
c) Describe the working of BCD to 7 segment decoder with truth table and circuit diagram.

Ans:- 02M circuit diagram, 01M explanation , 01M truth table

- BCD to **7** segment decoder is a combinational circuit that accepts 4 bit BCD input and generates appropriate 7 segment output.
- In order to produce the required numbers from 0 to 9 on the display the correct combination of LED segments need to be illuminated.
- A standard 7 segment LED display generally has 8 input connections, one from each LED segment & one that acts as a common terminal or connection for all the internal segments
- Therefore there are 2 types of display
    1. Common Cathode Display
    2. Common Anode Display

Circuit diagram:-

BCD to 7 segment decoder Using IC 7447



for normal Functioning $\overline{LT}$, $\overline{BI}/\overline{RBO}$ & $\overline{RBI}$ Should be connected to logic 1

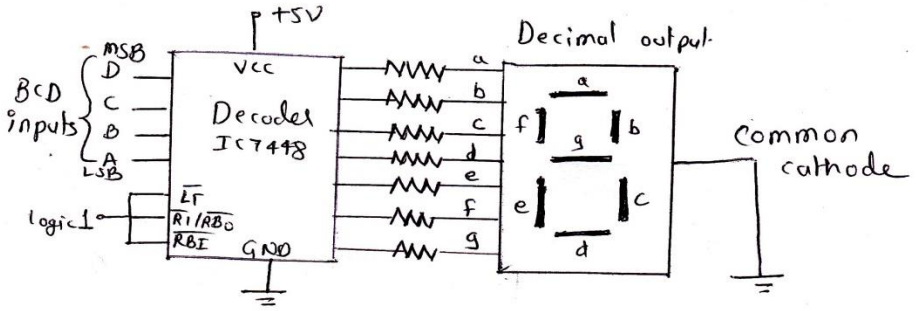
Observation Table

for seven segment decoder using common anode display

BCD Inputs				7 segment coded outputs							Display outputs
D	C	B	A	$\overline{a}$	$\overline{b}$	$\overline{c}$	$\overline{d}$	$\overline{e}$	$\overline{f}$	$\overline{g}$	
0	0	0	0	0	0	0	0	0	0	1	0
0	0	0	1	1	0	0	1	1	1	1	1
0	0	1	0	0	0	1	0	0	1	0	2
0	0	1	1	0	0	0	0	1	1	0	3
0	1	0	0	1	0	0	1	1	0	0	4
0	1	0	1	0	1	0	0	1	0	0	5
0	1	1	0	1	1	0	0	0	0	0	6
0	1	1	1	0	0	0	1	1	1	1	7
1	0	0	0	0	0	0	0	0	0	0	8
1	0	0	1	0	0	0	1	1	0	0	9

OR

BCD to 7 segment decoder Using IC 7448



BCD inputs				7 segment coded outputs							Display output
D	C	B	A	a	b	c	d	e	f	g	
0	0	0	0	1	1	1	1	1	1	0	
0	0	0	1	0	1	1	0	0	0	0	
0	0	1	0	1	1	0	1	1	0	1	
0	0	1	1	1	1	1	1	0	0	1	
0	1	0	0	0	1	1	0	0	1	1	
0	1	0	1	1	0	1	1	0	1	1	
0	1	1	0	0	0	1	1	1	1	1	
0	1	1	1	1	1	1	0	0	0	0	
1	0	0	0	1	1	1	1	1	1	1	
1	0	0	1	1	1	1	0	0	1	1	

d) Design 3-bit synchronous counter and draw O/P waveform (only logic diagram, table and waveforms expected).

Ans:- 01M truth table, 01M logical diagram, 01M design table, 01M waveform

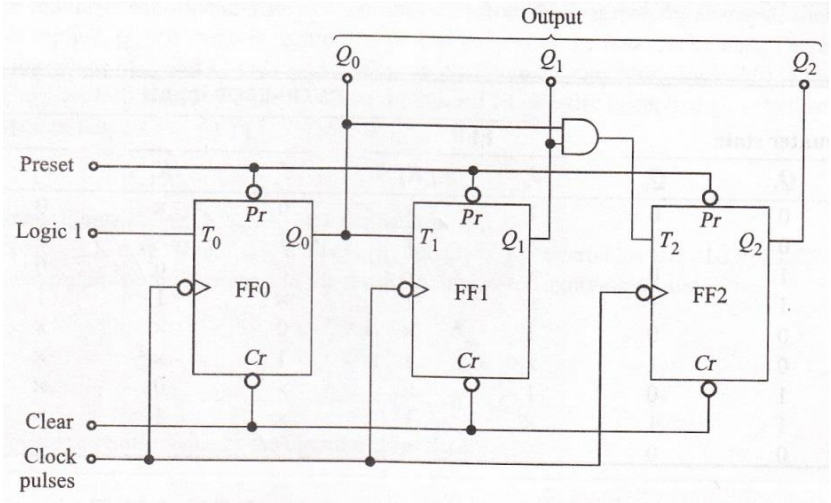
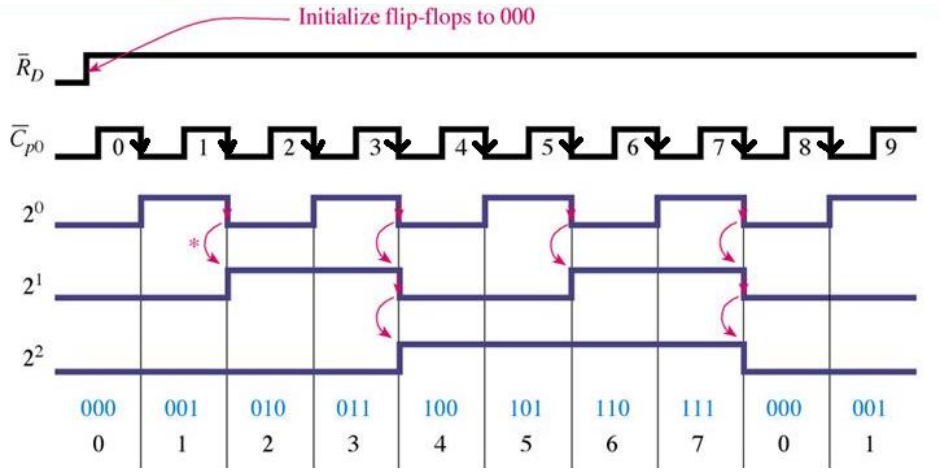


Table:-

Counter state			FLIP-FLOP inputs					
			FF0		FF1		FF2	
Q_2	Q_1	Q_0	J_0	K_0	J_1	K_1	J_2	K_2
0	0	0	1	×	0	×	0	×
0	0	1	×	1	1	×	0	×
0	1	0	1	×	×	0	0	×
0	1	1	×	1	×	1	1	×
1	0	0	1	×	0	×	×	0
1	0	1	×	1	1	×	×	0
1	1	0	1	×	×	0	×	0
1	1	1	×	1	×	1	×	1
0	0	0						



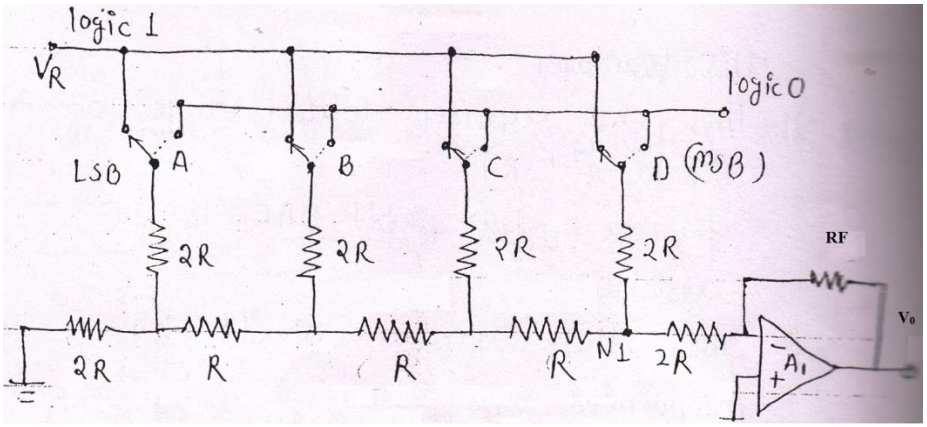
Truth table:-

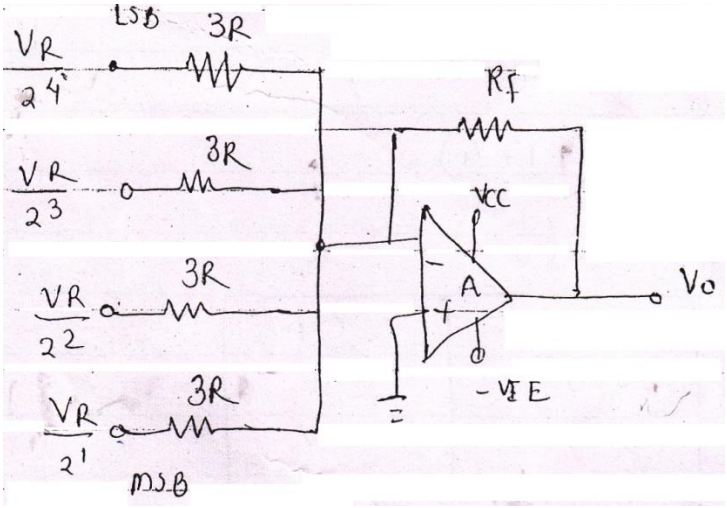
Input clock pulse	Q_2	Q_1	Q_0	Decimal equivalent count
↓	0	0	0	0
↓	0	0	1	1
↓	0	1	0	2
↓	0	1	1	3
↓	1	0	0	4
↓	1	0	1	5
↓	1	1	0	6
↓	1	1	1	7

	0	**0**	**0**	**0 (Sequence repeat)**

e) Draw the circuit diagram of 4-bit R-2R ladder DAC and obtain its output voltage expression.

Ans:- **02M voltage equation, 02M diagram**





Therefore output analog voltage V_0 is given by,

$$V_0 = -\left(\frac{Rf}{3R}\cdot\frac{VR}{2^4}b_0 + \frac{Rf}{3R}\cdot\frac{VR}{2^3}b_1 + \frac{Rf}{3R}\cdot\frac{VR}{2^2}b_2 + \frac{Rf}{3R}\cdot\frac{VR}{2^1}b_3\right)$$

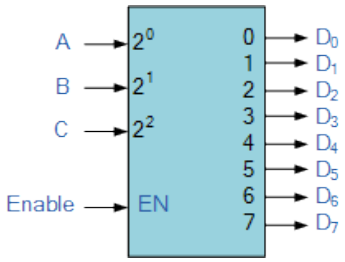
$$V_0 = -\left(\frac{Rf}{3R}\right)\left(\frac{VR}{2^4}\right)\left[8b_3 + 4b_2 + 2b_1 + b_0\right]$$

f) Design 3: 8 line decoder and give IC number for the same.

Ans:- **03M for designing , 01M for IC number**

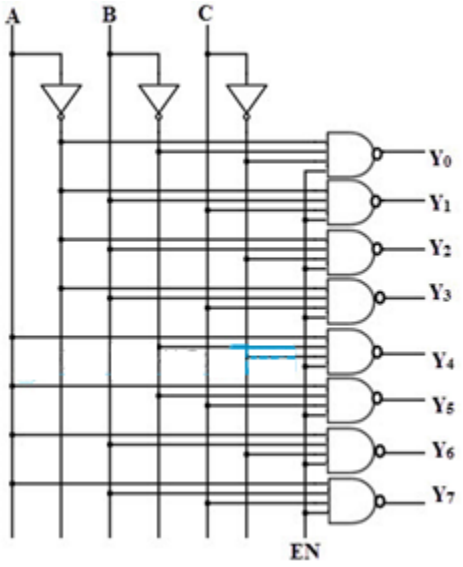
3:8 Decoder :-

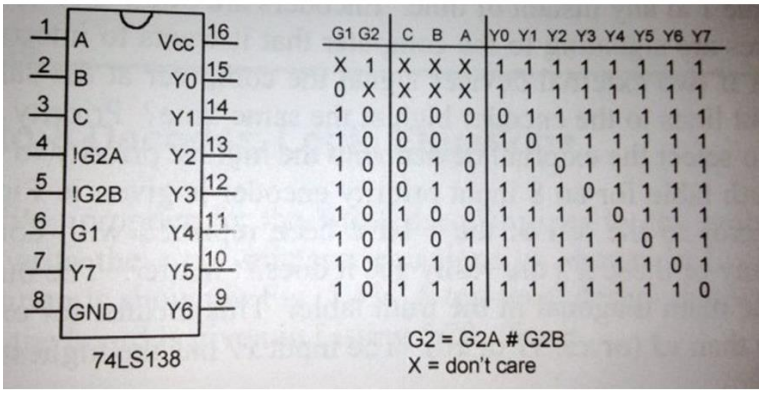
- A decoder generally decodes a binary value into a non-binary one by setting exactly one of its *n* outputs to logic "1".
- A binary decoder is a de-multiplexer with an additional data line that is used to enable the decoder. An alternative way of looking at the decoder circuit is to regard inputs A, B and C as address signals. Each combination of A, B or C defines a unique memory address.
- A decoder with 3 binary inputs (n = 3), would produce a 3-to-8 line decoder (TTL 74138)



74LS138 Binary Decoder

OR

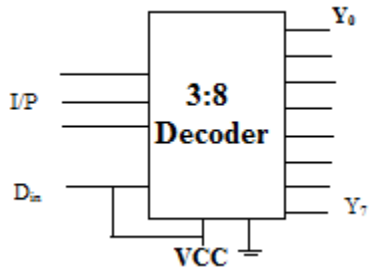




G1	G2	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	1	X	X	X	1	1	1	1	1	1	1	1
0	X	X	X	X	1	1	1	1	1	1	1	1
1	0	0	0	0	0	1	1	1	1	1	1	1
1	0	0	0	1	1	0	1	1	1	1	1	1
1	0	0	1	0	1	1	0	1	1	1	1	1
1	0	0	1	1	1	1	1	0	1	1	1	1
1	0	1	0	0	1	1	1	1	0	1	1	1
1	0	1	0	1	1	1	1	1	1	0	1	1
1	0	1	1	0	1	1	1	1	1	1	0	1
1	0	1	1	1	1	1	1	1	1	1	1	0

OR

De-multiplexer as a decoder



The decoder uses 3 selector inputs called A, B and C which together can make 8 possible combinations (2^3=8) and thus has 8 outputs (0,1,2,3,4,5,6 and 7).

Unlike the multiplexer the decoder does not required some gates in order to realize Boolen expression in the canonical SOP form.

IC number for 3:8 decoder is 74138