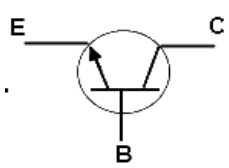
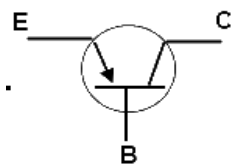
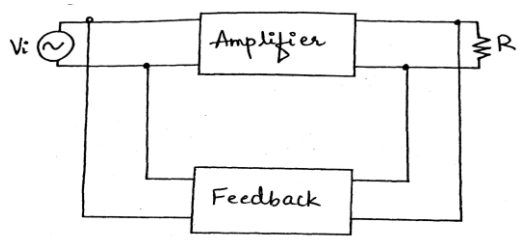
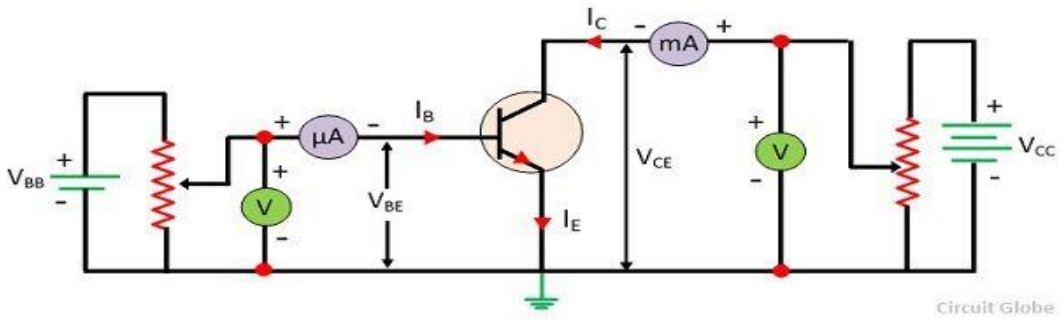
WINTER– 2018 EXAMINATION

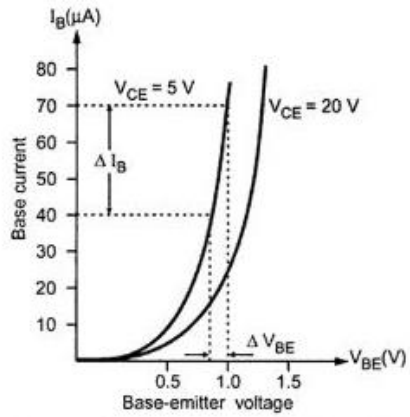
Model Answer **Subject Code:** 22346

Important Instructions to examiners:

1) The answers should be examined by key words and not as word-to-word as given in the model answer scheme.
2) The model answer and the answer written by candidate may vary but the examiner may try to assess the understanding level of the candidate.
3) The language errors such as grammatical spelling errors should not be given more Importance (Not applicable for subject English and Communication Skills)
4) While assessing figures, examiner may give credit for principal components indicated in the figure. The figures drawn by candidate and model answer may vary. The examiner may give credit for any equivalent figure drawn.
5) Credits may be given step wise for numerical problems. In some cases, the assumed constant values may vary and there may be some difference in the candidate's answers and model answer.
6) In case of some questions credit may be given by judgement on part of examiner of relevant answer based on candidate's understanding.
7) For programming language papers, credit may be given to any other program based on equivalent concept.

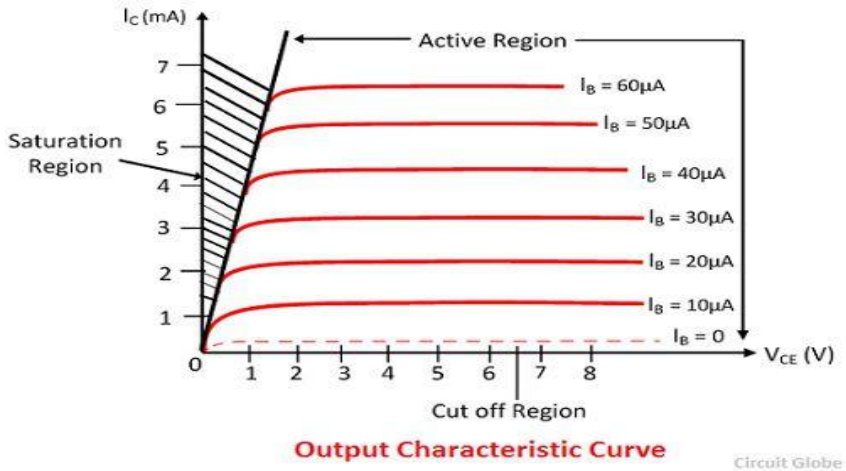
Q. No.	Sub Q. N.	Answer	Marking Scheme
1.		**Attempt any FIVE of the following:**	10 M
	a)	**State the types of BJT and draw their symbol.** **Ans:** BJTs are two types : PNP and NPN Transistor  NPN Transistor  PNP Transistor	01 M 01 M
	b)	**Define amplifier. State the types of coupling in multistage amplifier.** **Ans:** An amplifier is defined as a device, which produces a larger electrical output of similar characteristics than that of input parameters. **Types of coupling in multistage amplifier:** 1. Direct coupled amplifier 2. R.C coupled amplifier 3. Transformer coupled amplifier	01 M 01 M
	c)	**State Barkhausen's criteria for sustained oscillation.** **Ans:** Barkhausen's criteria states that: 1. An oscillator will operate at the frequency for which the total phase shift introduced as the signal proceeds from the input terminals through the amplifier and feedback network and back again to the input is precisely 0° or 360°. 2. At the oscillator frequency the magnitude of the product of open loop gain of the amplifier Av and the feedback factor β is equal to or greater than unity ($\beta Av \geq 1$).	02 M

	d)	**List the types of feedback connection. Identify the feedback connection given in Figure No.1.**  **Figure No.1** **Ans:** **Types of feedback connection:** 1. Voltage series feedback connection 2. Voltage shunt feedback connection 3. Current series feedback connection 4. Current shunt feedback connection Figure No.1**.** is Voltage shunt feedback connection	**01 M** **01 M**
	e)	**State the need of wave shaping circuits.** **Ans:** In most of the electronic circuits, it becomes essential to modify the shape of the signal for certain reasons, It is sometimes to shift the dc level of the input signal while keeping the signal shape unchanged. This can be achieved by using some kind of wave shaping circuits.	**02 M**
	f)	**Define the following terms :** **(i) Load regulation** **(ii) Line regulation** **Ans:** (i) Load regulation: Load regulation is defined as the ratio of change in output voltage to the change in load current with constant input voltage. (ii) Line regulation: Line regulation is defined as the ratio of change in output voltage to the input voltage with load (R_L).	**01 M** **01 M**
	g)	**State the functions of rectifier and filter circuits in regulated power supply.** **Ans:** Functions of rectifier: It converts the ac voltage into a pulsating dc voltage. Functions of Filter: The ripple in the pulsating dc is reduced by the filter and the output is a smooth dc voltage.	**01 M** **01 M**
2.		**Attempt any <u>THREE</u> of the following:**	**12 M**
	a)	**Draw the circuit diagram of transistor in CE configuration and draw input and output characteristics.** **Ans:**  **Circuit diagram of transistor in CE configuration**	**02 M**



Input characteristics of the transistor in CE configuration

01 M

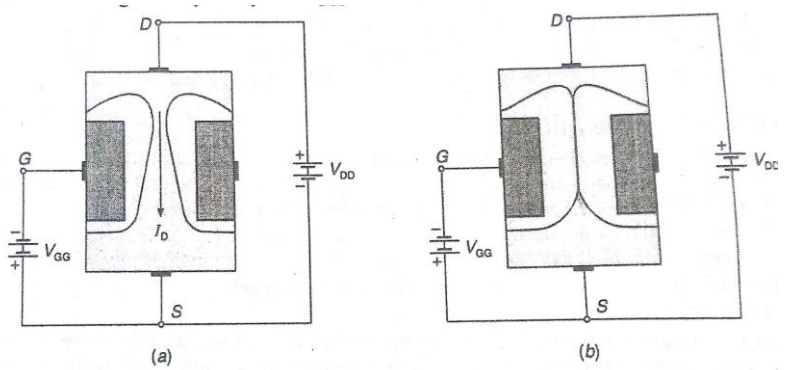


Output Characteristic Curve

01 M

b) Explain the working of n-channel JFET with neat diagram.

Ans:



02 M

When the gate to sour voltage (V_{GS}) , if applied by a dc supply V_{GG} and increased above zero as shown in fig a the reverse bias voltage across the gate source junction is increased. As result of this, the depletion regions are widened. This reduces the effective width of the channel and therefore controls the flow of drain current through the channel. When the gate to source voltage (V_{GS}) is increased further a stage is reached which two depletion region touch each other as shown in fig b. At this gate to source voltage the channel is completely blocked or pinched off and drain current is reduced to zero. The gate to source voltage (V_{GS}) at which the drain current is reduced to zero(or completely cut off) is called pinch off voltage.

02 M

c) Compare class A, class B and class C power amplifiers on the basis of: **04 M**

(i) Conduction angle of collector current
(ii) Position of Q-point
(iii) Distortion in output voltage
(iv) Efficiency

Ans:

Parameter	class A	class B	class C
Conduction angle of collector current	360° or full cycle	180° or half cycle	Less than 180°
Position of Q-point	At the center of load line	In the cut off region (on the x- axis)	Just above the cut off (below x-axis)
Distortion in output voltage	No distortion	More than class A (Cross over)	Low
Efficiency	Lowest (25% to 50%)	Higher (78.5%)	Very high (95%)

d) Define the following parameters of JFET **03 M**

(i) DC drain resistance (rd)
(ii) Amplification factor (μ)
(iii) Transdconductance (gm)
State the relation between μ rd and gm.

Ans:

(i) DC drain resistance (rd) : It is defined as ratio of drain to source voltage (ΔV_{DS}) to drain current (ΔI_D) for constant gate to source voltage (V_{GS}).
rd = $\Delta V_{DS}/\Delta I_D$ keeping constant V_{GS}

(ii) Amplification factor (μ): It is given by the ratio of small change in drain to source voltage (ΔV_{DS}) to the corresponding change in gate to source voltage (ΔV_{GS}) for constant drain current (I_D).
$\mu = \Delta V_{DS} / \Delta V_{GS}$ keeping I_D constant.

(iii)Transdconductance (gm): It is given by the ratio of small change in drain current (ΔI_D) to the corresponding change in gate to source voltage (ΔV_{GS}) for constant drain to source voltage (V_{DS})
gm = $\Delta I_D/\Delta V_{GS}$ keeping Constant V_{DS}

Relation between μ, gm and rd: **01 M**

From definitions, $\mu = \Delta V_{DS} / \Delta V_{GS}$ …… i)
gm = $\Delta I_D / \Delta V_{GS}$…… ii)
rd = $\Delta V_{DS} / \Delta I_D$ …… … iii)
Multiply and Divide eq i) by ΔI_D
$\mu = (\Delta I_D / \Delta V_{GS}) * (\Delta V_{DS} / \Delta I_D)$
i.e μ =gm * rd (from ii & iii)

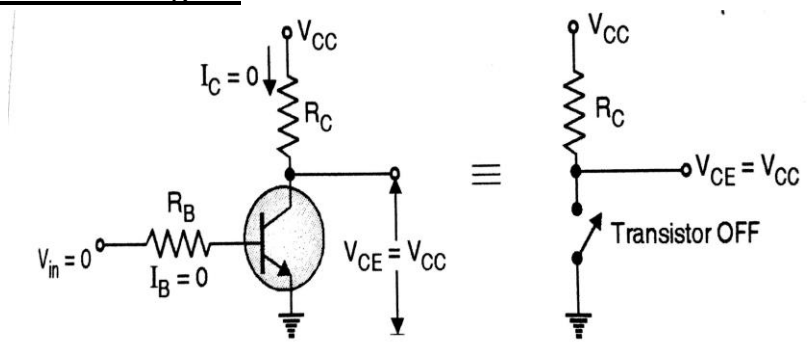
3. Attempt any <u>THREE</u> of the following: **12 M**

a) Explain the operation of transistor as a switch with neat diagram.

Ans:(Diagram -02 , Explanation 02)

The transistor can be used for two types of application viz. amplification and switching. For the amplification, transistor is biased in its active region. Whereas for switching applications it is biased to operate in the saturation (full ON) or cut off (full OFF) region.

a. Transistor in cut- off region:

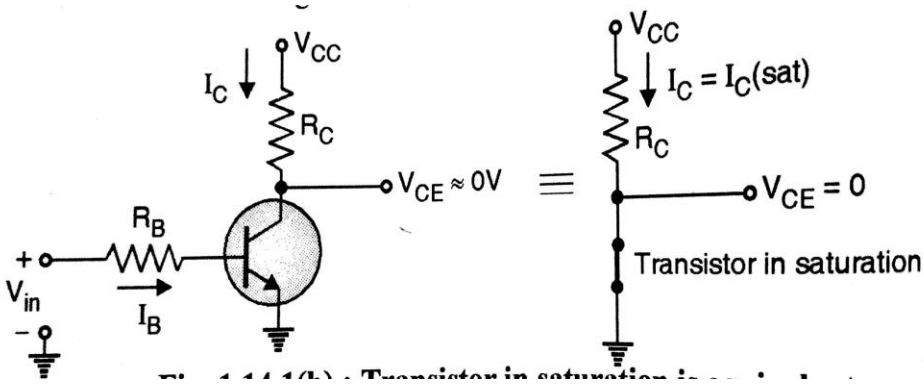


04 M

In the cut –off region both the junction of a transistor are reverse biased and very small reverse current flows through the transistors.

- The voltage drop across the transistor (VCE) is high. Thus, in the cut off region the transistor is equivalent to an open switch as shown in figure.

Transistor in the saturation region:

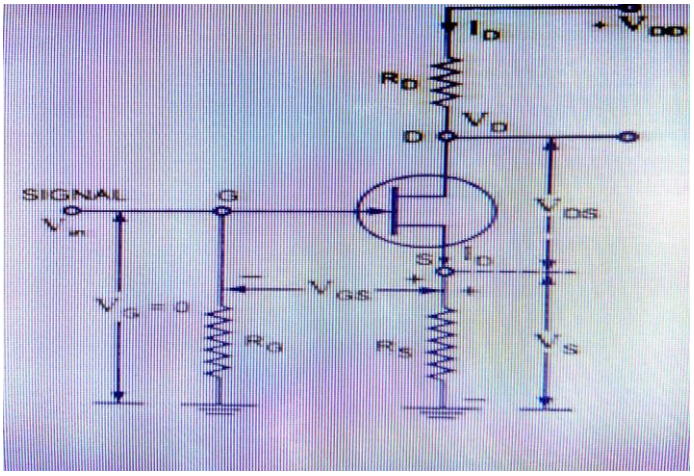


When Vin is positive a large base current flows and transistor saturates.

- In the saturation region both the junctions of a transistor are forward biased. The voltage drop across the transistor (VCE) is very small, of the order of 0.2 V to 1V depending on the type of transistor and collector current is very large.
- In saturation the transistor is equivalent to a closed switch.

b) Describe the self biased method for FET with neat diagram.

Ans:



02 M

In this circuit there is only one drain supply and no gate supply.
The gate terminal is connected through resistor RG to the ground.
The source terminal is connected through resistor RS to the ground.
{NOTE: In JFET input PN junction between gate & source is always reverse bias, due to this input resistance of JFET is very high. Due to this input gate current I_G = zero. Hence if resistor R_G is connected in series with gate terminal, voltage drop across R_G is zero as $V_{RG} = I_G R_G = 0$}

- $V_G = I_G R_G = 0$
- $V_{GS} = V_G - V_S$
  $= -V_S$

APPLY KVL TO INPUT LOOP
$V_{GS} + I_D R_S = 0$
$V_{GS} = - I_D R_S$

- $I_D = I_{DSS}\{1- V_{GS} / V_P\}^2$ Shockley"s equation
- APPLY KVL TO OUTPUT LOOP

$V_{DD} - I_D R_D - V_{DSQ} – I_D R_S = 0$
$V_{DSQ} = V_{DD} - I_D R_D – I_D R_S$
$= V_{DD} - I_D [R_D + R_S]$

02 M

c) Draw and explain UJT relaxiation oscillator with circuit diagram.
Ans:

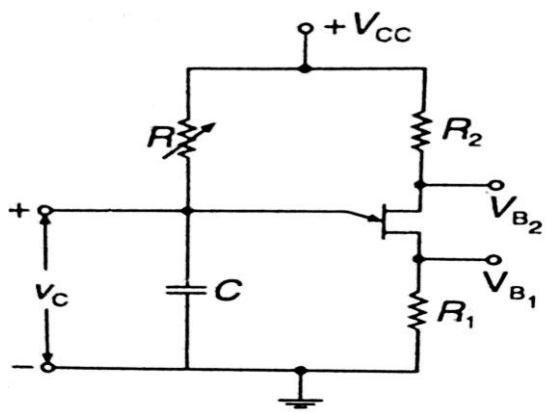


Fig.1

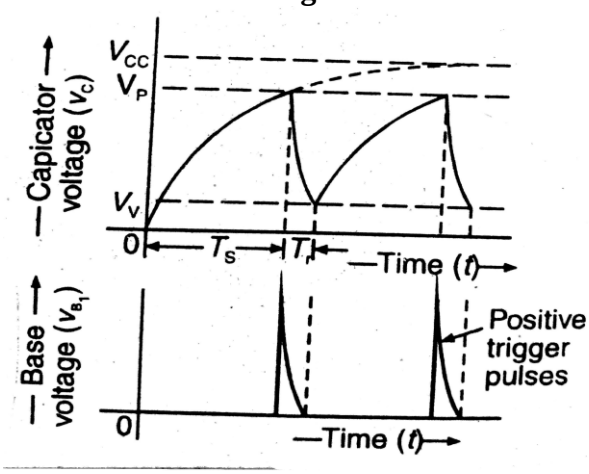


Fig 2

02 M

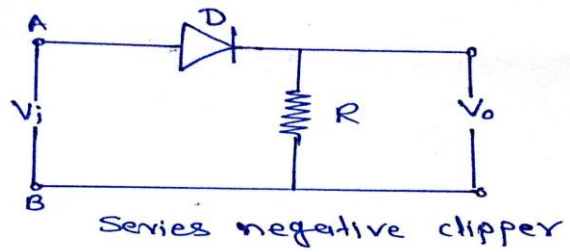
When the supply voltage (V_{CC}) is switched ON, the capacitor (C) charges through resistor (R), till the capacitor voltage reaches the voltage level (Vp) which is called peak point voltage. At this voltage, the unijunction transistor turns ON.As result of this, the capacitor (C) discharges rapidly through resistor (R_1). When that capacitor voltage drops to level V_V (called valley – point voltage) the unijunction transistor switches OFF allowing the capacitor (C) to charge again. In fig 2 the collector voltage and the base 1 voltage waveform during capacitor charging and discharging interval. The voltage developed at base 1 terminal is in the form of narrow pulses commonly known as trigger pulses. The similar pulses but opposite polarity are also available at the base terminal of the unijunction transistor. **02 M**

d) The negative half cycles to be clipped from the given input signal. (V_{in} = 10 sin wt). Name and draw the circuit with input –output waveforms.

Ans:

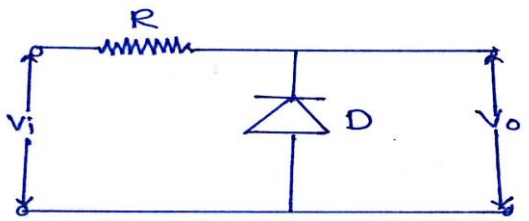
Negative clipper, the negative half cycles of the input voltage will be removed. The circuit arrangements for a negative clipper are illustrated in the figure given below. **01 M**

Circuit diagram:

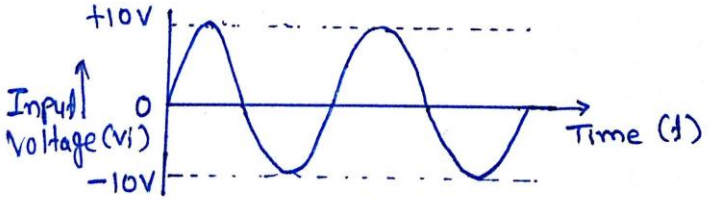


Series negative clipper

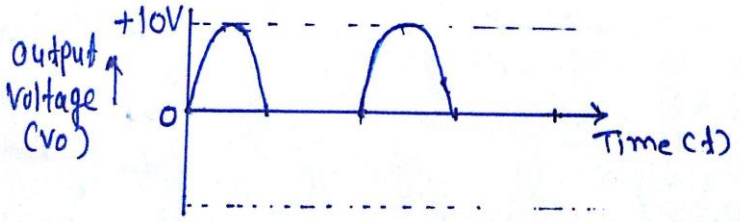
OR **01 M**



Shunt negative clipper



Input waveforms **02 M**

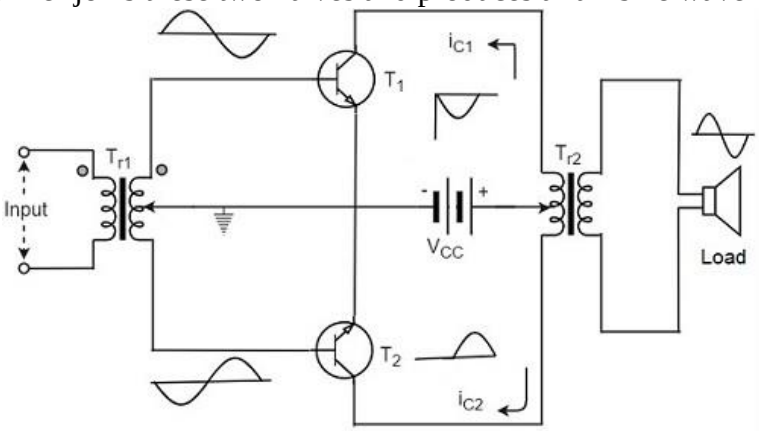


output waveforms

4.		**Attempt any <u>THREE</u> of the following:**	**12 M**
	a)	**Define α and β of transistor and derive the relation between α and β.** **Ans:** Alpha (α): It is a large signal current gain in common base configuration. It is the ratio of collector current (output current) to the emitter current (input current). Beta (β): It is a current gain in the common emitter configuration. It is the ratio of collector current (output current) to base current (output current). **Relation between α& β:** We know that emitter current (I_E) of a transistor is the sum of its base current (I_B) and collector current (I_C). *i.e.*, $I_E = I_B + I_C$ Dividing the above equation on both sides by I_C, $\frac{I_E}{I_C} = \frac{I_B}{I_C} + 1$ Since $I_C/I_E = \alpha$ and $I_C/I_B = \beta$ therefore $\frac{1}{\alpha} = \frac{1}{\beta} + 1 = \frac{1+\beta}{\beta}$ $\therefore \quad \alpha = \frac{\beta}{\beta+1}$ The above expression may be written as $\alpha(\beta+1) = \beta$ $\alpha \cdot \beta + \alpha = \beta$ $\alpha = \beta - \alpha \cdot \beta = \beta(1-\alpha)$ $\therefore \quad \beta = \frac{\alpha}{1-\alpha}$	**01 M** **01 M** **02 M**
	b)	**Find the values of V_{DS} and V_{GS} for given values of I_D = 5mA, V_{DD} =10V, R_D =1kΩ and R_S = 500 Ω** **Ans:** Given I_D = 5mA, V_{DD} =10V, R_D =1kΩ and R_S = 500 Ω $V_{DS} = V_{DD} - I_D [R_D + R_S]$ $= 10 - 5 \times 10^{-3} \times [1\times10^3 + 500]$ $\mathbf{V_{DS} = 2.5V}$ $\mathbf{V_{GS}} = - I_D R_S$ $= - 5 \times 10^{-3} \times 500$ $\mathbf{V_{GS} = - 2.5V}$	**02 M** **02 M**
	c)	**Draw the circuit diagram of class B push pull amplifier and describe its working.** **Ans:** **<u>Working :</u>** • When there is no input signal both the transistor T_1 and T_2 are cut-off. Hence no current is drawn from V_{CC} supply. Thus there is no power wasted in standby the power dissipation in both transistor is practically zero. • During positive half cycle the base of T_1 is positive and T_2 is negative. As a result of this T_1 conduct, while the transistor T_2 is OFF. And at the output half cycle is obtained. • During negative half cycle, T_1 turns OFF and T_2 conducts, and another half cycle is obtained at the output. At any instant only one transistor in the circuit is conducting. Each	**02 M**

transistor handles one half of the input signal.

- Then output transformer joins these two halves and produces a full-sine wave in the load.



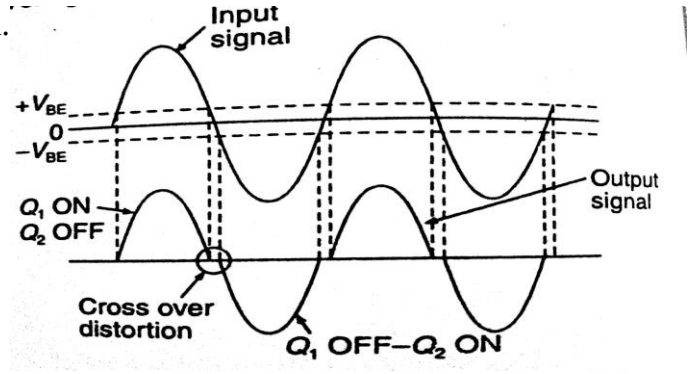
02 M

d) Explain what is cross – over distortion. How it is overcome, show with circuit diagram?

Ans:

In a class B push pull amplifier are biased at cut-off. It means that when the dc bias voltage is zero, the input signal voltage must exceed that barrier voltage before a transistor conducts. In other words, a transistor does not conduct, until the input signal voltage exceeds 0.7 V for silicon and 0.3V for germanium transistors. Because of this, there is time interval between the positive and negative alternation of the input signal when neither transistor is conducting as shown in figure. The resulting distortion in the output signal is quite common and is called crossover distortion.

02 M



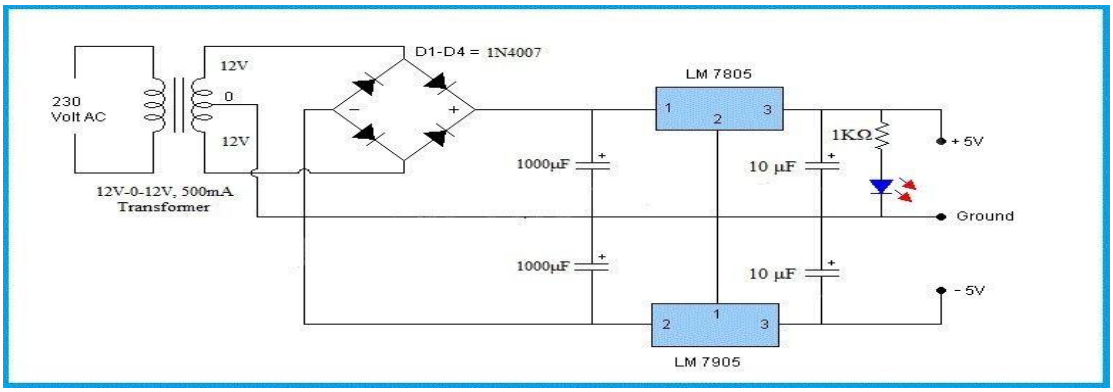
01 M

The crossover distortion may be avoided by applying a slight forward bias to the base emitter junction of both the transistors of the amplifier circuit. It causes the transistor conduct immediately, when the ac input signal is applied. The application of slight forward bias shifts the Q-point slightly above the cut-off.

01 M

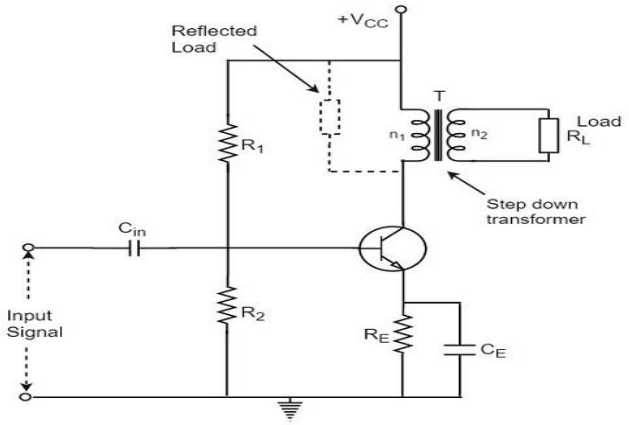
e) Design regulated dual power supply for ± 5V using regulator IC's.

Ans:



04 M

5.		**Attempt any TWO of the following:**	**12 M**
	a)	**Explain thermal runway in transistor. How can it be avoided? List any two methods of biasing of transistor.** **Ans:** **Concept of thermal runaway:** 1. The reverse saturation current in semiconductor devices changes with temperature. The reverse saturation current approximately doubles for every 10° rise in temperature. 2. As the leakage current of transistor increases, collector current (Ic) increases 3. The increase in power dissipation at collector base junction. 4. This in turn increases the collector base junction causing the collector current to further increase. 5. This process becomes cumulative & amp; it is possible that the ratings of the transistor are exceeded. If it happens, the device gets burnt out. This process is known as "Thermal Runaway". **Thermal Runaway can be avoided :** 1. Using stabilization circuitry 2. Use heat sink **Biasing methods of transistor:** 1. Fixed bias. 2. Base bias with emitter feedback. 3. Base bias with collector feedback 4. Voltage divider bias. 5. Emitter bias	**02M** **02M** **02M**
	b)	**Draw circuit diagram and explain the operation of transformer coupled class A power amplifier. State its advantages.** **Ans:** The overall efficiency of a direct coupled class-A amplifier does not exceed 25%. In order to minimize those effects, the transformer coupled class A power amplifier has been introduced. This is similar to the normal amplifier circuit but connected with a transformer in the collector load. Here R_1 and R_2 provide potential divider arrangement. The resistor Re provides stabilization, C_e is the bypass capacitor and R_e to prevent a.c. voltage. The transformer used here is a step-down transformer. The high impedance primary of the transformer is connected to the high impedance collector circuit. The low impedance secondary is connected to the load (generally loud speaker). The transformer used in the collector circuit is for impedance matching. R_L is the load connected in the secondary of a transformer. R_L' is the reflected load in the primary of the transformer. The number of turns in the primary is n_1 and the secondary are n_2. Let $V_1$and V_2 be the primary and secondary voltages and I_1 and I_2 be the primary and secondary currents respectively. If the peak value of the collector current due to signal is equal to zero signal collector current, then the maximum a.c. power output is obtained. So, in order to achieve complete amplification, the operating point should lie at the center of the load line. The operating point obviously varies when the signal is applied. The collector voltage varies in opposite phase to the collector current. The variation of collector voltage appears across the primary of the transformer.	**02 M**



02 M

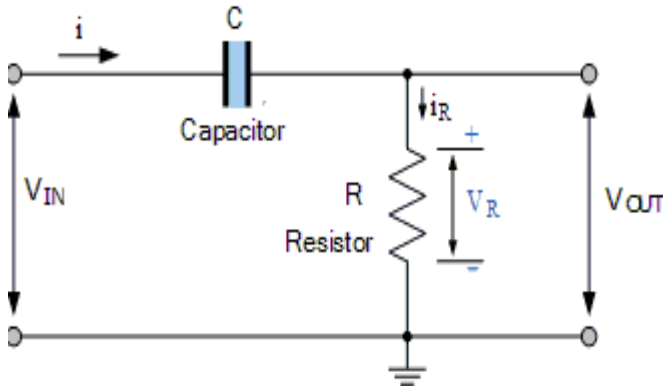
Advantages :

1. Maximum power transfer to load is possible due to the impedance matching via transformer.
2. The dc biasing current does not flow through the load some power saving takes place.
3. Higher efficiency than the direct coupled amplifier.
4. Gain is high.

02 M

c) Draw circuit diagram of RC differentiator for a sinusoidal input. Derive the expression for output voltage. In case, if same circuit is connected to a square wave input, draw the output waveform.

Ans:



02 M

Output waveforms for square wave input:

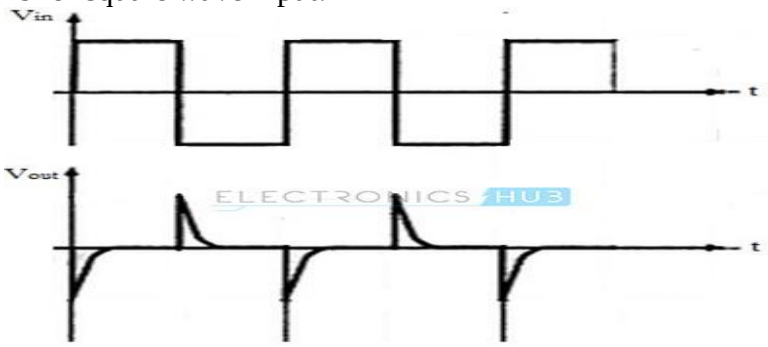


Fig: Input and Output waveforms for Square wave

02 M

$$v_o \propto \frac{dv_i}{dt}$$

$$= k \cdot \frac{dv_i}{dt}$$

where k is a constant of proportionality.

A differentiating circuit may be realised by a simple RC series circuit as shown i
In this circuit, the output is taken across the resistor (R). The circuit is designed in s
reactance of the capacitor ($X_C = 1/2\pi f_C$) is very large as compared to the value of re

$$X_C >> R$$

$$\frac{1}{2\pi f_C} >> R$$

or

$$\frac{1}{2\pi RC} >> f$$

where f = Frequency of the input signal, and
C = Value of capacitance of the capacitor.

We know that the time period of the input signal,

$$T = \frac{1}{f}$$

∴ Equation (i) may be rewritten as

$$\frac{1}{2\pi RC} << \frac{1}{T}$$

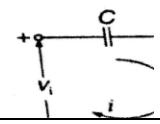
$$2\pi RC << T$$

or

$$\tau << T$$

where $\tau = RC$ is called time constant of the circuit.

It is evident from equation (ii) that if time constant of the RC circuit ($i.e.$, $\tau =$
smaller than the time period of the input signal waveform,
then the output of the circuit.



$$v_o = R \cdot C \cdot \frac{dv_i}{dt}$$

02 M

6. **Attempt any TWO of the following:** **12 M**

a) **A phase shift oscillator has R = 220kΩ and C = 500pF. Calculate the frequency of sine wave generated by the oscillator. State the application of RC oscillators.**

Ans: Given : R = 220kΩ , C = 500pF

Frequency f = $\frac{1}{2\pi\sqrt{6}\,RC}$

$$\frac{1}{2\pi\sqrt{6} \times 220 \times 10^3 \times 500 \times 10^{-12}}$$

= 590.67 Hz

f = 590.67 Hz

04 M

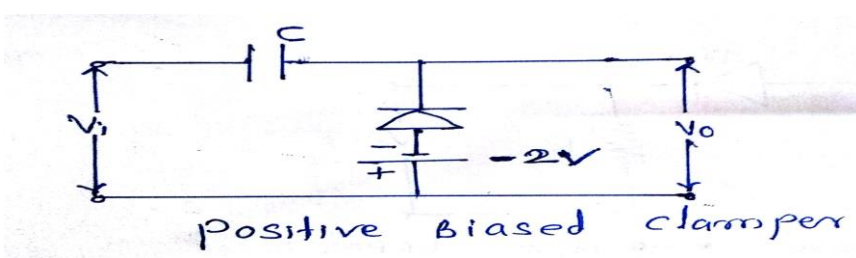
Application of RC oscillators:

1. For generating signals in audio frequency range
2. Variable frequency range.
3. Function generators / signal generators use in laboratories.

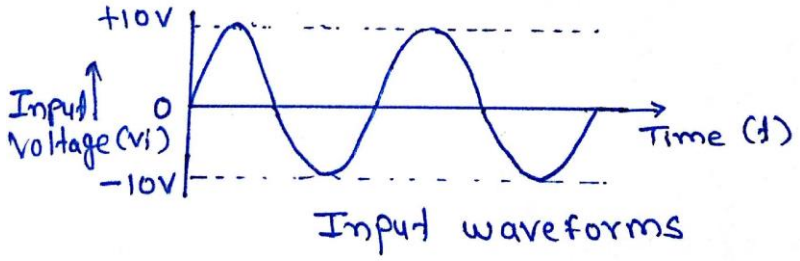
02 M

b) **A dc level of + 2V is to be added to the given input signal (V_i = 10 sin wt). Explain the working principle of this application with circuit diagram and input- output waveforms.**

Ans:

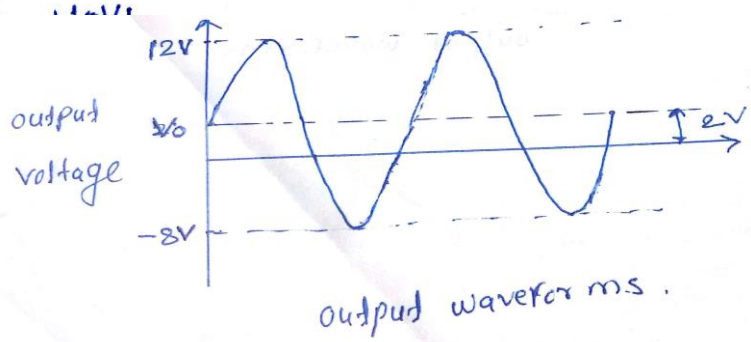


02 M



Input waveforms

01 M



output waveforms.

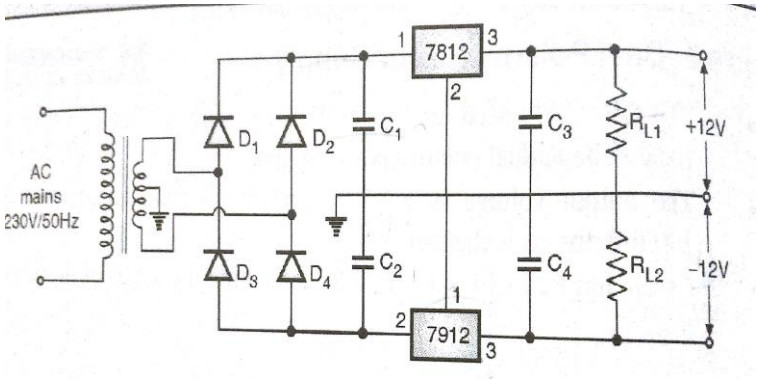
Working: **01 M**

During negative half cycle: During the negative half cycle, the battery voltage reverse biases the diode when the input supply voltage is less than the battery voltage. As a result, the signal appears at the output. When the input supply voltage becomes greater than the battery voltage, the diode is forward biased by the input supply voltage and hence allows electric current through it. This current will flows to the capacitor and charges it.

During positive half cycle: During the positive half cycle, the diode is reverse biased by both input supply voltage and the battery voltage. As a result, the signal appears at the output. The signal appeared at the output is equal to the sum of the input voltage and capacitor voltage. **02 M**

c) Draw the circuit diagram of DC regulated dual power supply for ± 12Vusing IC's 78XX and 79XX. State the necessity of regulated power supply.

Ans:



04 M

Necessity of regulated power supply: The major disadvantage of a power supply is that the output voltage changes with the variations in the input voltage or The D.C output voltage of the rectifier also increase similarly, In many electronic applications, it is desired that the output voltage should remain constant regardless of the variations in the input voltage or load. In order to get ensure this; a voltage stabilizing device called voltage regulator is used **02 M**