WINTER– 18 EXAMINATION

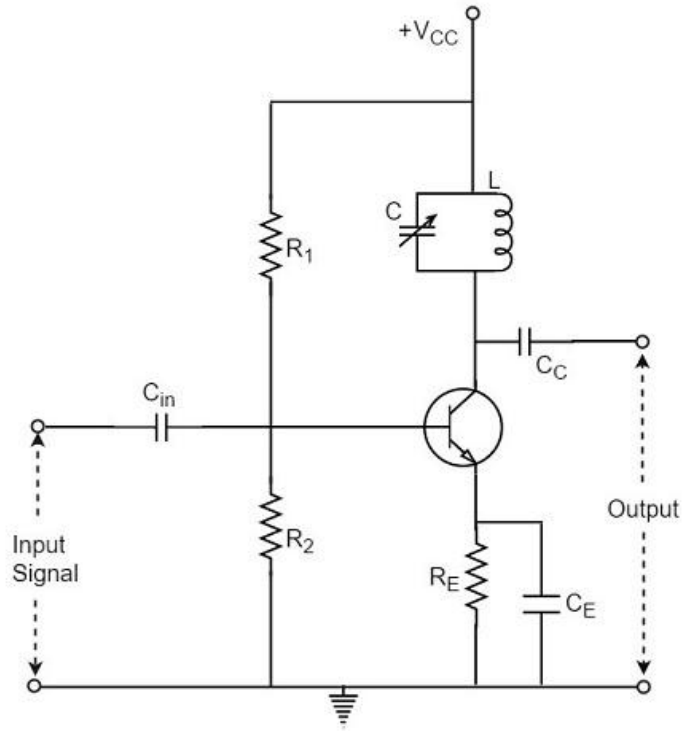
Subject Name: Electronic Devices and Circuits **Model Answer Subject Code:** 17319

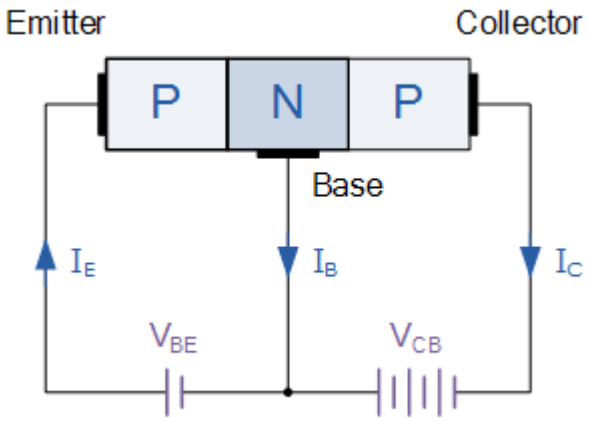
Important Instructions to examiners:

1) The answers should be examined by key words and not as word-to-word as given in themodel answer scheme.
2) The model answer and the answer written by candidate may vary but the examiner may tryto assess the understanding level of the candidate.
3) The language errors such as grammatical, spelling errors should not be given moreImportance (Not applicable for subject English and Communication Skills.
4) While assessing figures, examiner may give credit for principal components indicated in thefigure. The figures drawn by candidate and model answer may vary. The examiner may give credit for anyequivalent figure drawn.
5) Credits may be given step wise for numerical problems. In some cases, the assumed constantvalues may vary and there may be some difference in the candidate's answers and model answer.
6) In case of some questions credit may be given by judgement on part of examiner of relevant answer based on candidate's understanding.
7) For programming language papers, credit may be given to any other program based on equivalent concept.

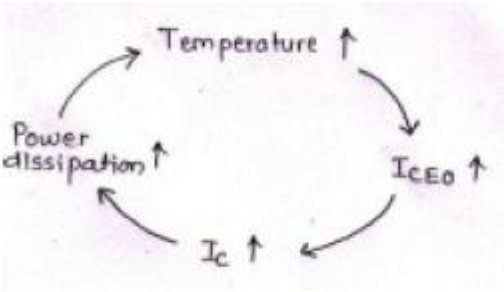
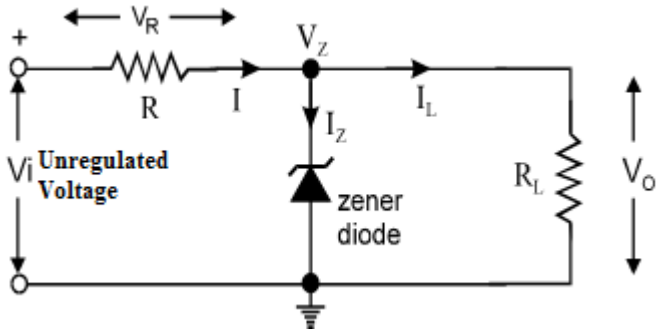
Q. No.	Sub Q. N.	Answers	Marking Scheme
1	**(A)**	**Attempt any SIX :**	**12- Total Marks**
	(a)	**State any four applications of transistor.**	**2M**
	Ans:	Application: 1) Amplifier 2) Switching application 3) Oscillators 4) Wave shaping circuits 5) Logic circuits 6) Timer and Multivibrator	**Any Four applicati on-1/2 each**

		7) Delay circuits	
	(b)	**Define term stability factor.**	**2M**
	Ans:	Definition of stability factor: It is defined as the rate of change of collector current I_C with respect to the collector base leakage current I_{co}, keeping both the current I_B and the current gain β constant. $S = \frac{\partial I_C}{\partial I_{co}} = \frac{dI_C}{dI_{co}} = \frac{\Delta I_C}{\Delta I_{co}}$	**Definitio n-2M**
	(c)	**Define gain and bandwidth.**	**2M**
	Ans:	**Gain:** It is the ratio of output quantity to the input quantity. **Bandwidth**: It is defined as the range (band) of frequency over which the gain is constant. **(Or)** It is the range of frequency over which the gain is greater than 70.7% of the maximum gain possible.	**Definitio n-1M each** **Note: Any other suitable definitio n also can be consider**
	(d)	**Which type of MOSFET is called Normally ON MOSFET"? Why?**	**2M**
	Ans:	**DMOSFET** is called Normally ON MOSFET. In DMOSFET already channel is present and at Vgs = 0v, drain current Id=Idss i.e. drain to source saturation current is flowing.	**Identify type-1M** **Reason-1M**
	(e)	**Sketch the single tuned amplifier.**	**2M**

	Ans:		**Neat sketch-2M**
	(f)	**List the types of power amplifier.**	**2M**
	Ans:	Types of Power amplifier: 1) Class A power amplifier 2) Class B power amplifier 3) Class AB power amplifier 4) Class C power amplifier	**1/2 M each**
	(g)	**State 2 advantages of JFET over BJT.**	**2M**
	Ans:	Advantages of JFET over BJT: 1) High input impedance 2) Better thermal stability	**Any two advantges-1M each**

		3) Produce less noise 4) Smaller than BJT 5) Rugged in construction and simpler to fabricate 6) High degree of isolation between Input and Output.	
	(h)	**Define intrinsic standoff ratio.**	**2M**
	Ans:	It is defined as the ratio of the R_{B1} (base resistance 1) to the inter-base resistance R_{BB}. $\eta = \frac{R_{B1}}{R_{B1} + R_{B2}}$ $\eta = \frac{R_{B1}}{R_{BB}}$	**Definition -2M**
	(B)	**Attempt any TWO :**	**08- Total Marks**
	(a)	**Explain the operating principle of PNP transistor.**	**4M**
	Ans:		**Diagram -2M** **Operating principle -2M**

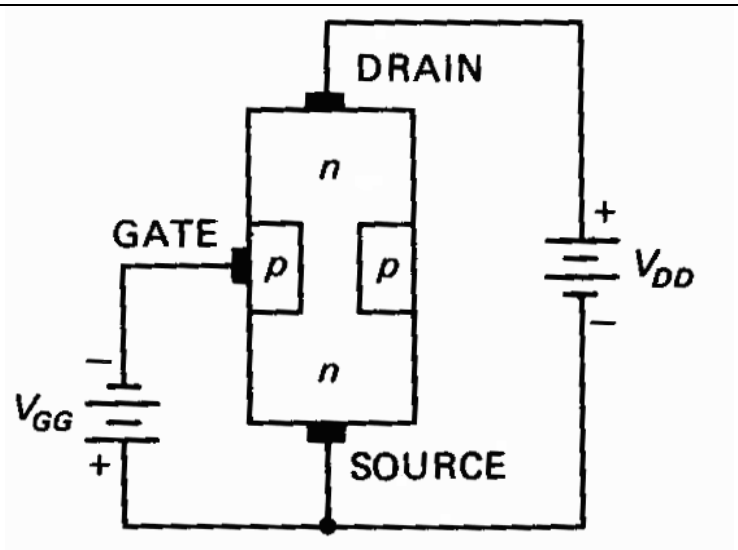
		The circuit connection of PNP transistor with supply voltages is as shown above. The emitter-base junction is connected as forward bias. Due to this the emitter pushes the holes from the P type emitter region across the emitter-base junction into the base region. These holes constitute the emitter current I_E. When these holes move into the N-type semiconductor material or base, they combined with the electrons. The base of the transistor is thin and very lightly doped. Hence only a few holes combined with the electrons and the remaining are moved towards the wide and medium doped P type collector region. This is the base current I_B. The collector base region is connected in reverse bias. The holes which collect around the depletion region when coming under the impact of negative polarity collected or attracted by the collector. This develops the collector current I_C. This is how a PNP transistor operates.	
	(b)	**What is thermal runaway in transistor? How it can be avoided?**	**4M**
	Ans:	**Concept of thermal runaway:** 1.We know that IC = β IB + (1+ β) ICO Where I_{CO} is the leakage current and I_{CO} is strongly dependent on temperature. 2. Leakage current approximately doubles for every 10^0 C rise in temperature. 3 As the leakage current of transistor increases, collector current (Ic) increases (1+ β) times. 4. This increases the power dissipation at collector base junction. 5. This in turn increases the temperature of the collector base junction which will increase the number of minority carriers. 6. So I_{CO} further increases causing the collector current to increase further. 7. This effect is cumulative and in a fraction of a second Ic becomes large causing transistor	**Thermal runaway -2M** **Techniques to avoid thermal runaway -2M**

		to burn up. This self-destruction of an unstabilized transistor is known as Thermal Runaway.  **Thermal runaway can be avoided by :** 1) Using stabilization circuitry 2) Heat sink	
	(c)	**Explain how Zener diode is used as voltage regulator.**	**4M**
	Ans:	**Circuit Diagram:**  For proper operation, the input voltage Vi must be greater than the Zener voltage Vz. This ensures that the Zener diode operates in the reverse breakdown condition. The unregulated input voltage Vi is applied to the Zener diode. Suppose this input voltage exceeds the Zener voltage. This voltage operates the Zener	**Diagram -2M** **Explanation-2M**

		diode in reverse breakdown region and maintains a constant voltage, i.e. Vz = Vo across the load in spite of input AC voltage fluctuations or load current variations. The input current is given by, **$I = (V_i - V_z) / R = (V_i - V_o) / R$** The input current I the sum of Zener current Iz and load current IL. ***$I = I_z + I_L$*** ***OR*** ***$I_z = I - I_L$*** As the load current increase, the Zener current decreases so that the input current remains constant. According to Kirchhoff's voltage law, the output voltage is given by, ***$Vo = Vi - I . R$*** As the input current is constant, the output voltage remains constant. Similarly if the load current decreases the output voltage remains constant. This circuit is also correct for the changes in input voltage. As the input voltage increases, more Zener current will flow through the Zener diode. This increases the input voltage I, and also the voltage drop across the resistor R, but the load voltage Vo would remain constant. Similarly, if the decrease in input voltage is not below Zener voltage, the output voltage remains constant. Thus, a Zener diode acts as a voltage regulator and the fixed voltage is maintained across the load resistor RL.	

Q. No.	Sub Q. N.	Answers	Marking Scheme

2		Attempt any FOUR :	16- Total Marks
	(a)	**Define α and β of transistor and derive the relation between them.**	4M
	Ans:	**Alpha (α):** It is a large signal current gain in common base configuration. It is the ratio of collector current (output current) to the emitter current (input current). **Beta (β):** It is a current gain in the common emitter configuration. It is the ratio of collector current (output current) to base current (output current). **Relation between α& β:** Current gain (α) of CB configuration $= \frac{I_C}{I_E}$ Current gain of (β) of CE configuration $= \frac{I_C}{I_B}$ We know that ; $I_E = I_B + I_C$.....(1) Dividing equation (1) by I_C $\frac{I_E}{I_C} = \frac{I_B}{I_C} + \frac{I_C}{I_C}$ Therefore $\frac{1}{\alpha} = \frac{1}{\beta} + 1$ [since $\alpha = \frac{I_C}{I_E}$, $\beta = \frac{I_C}{I_B}$] Therefore $\frac{1}{\alpha} = \frac{1+\beta}{\beta}$ $\alpha(1 + \beta) = \beta$ $\alpha + \alpha\beta = \beta$ $\alpha = \beta - \alpha\beta$ $\alpha = \beta(1 - \alpha)$ Therefore $\beta = \frac{\alpha}{1-\alpha}$ OR $\alpha = \frac{\beta}{1+\beta}$ Note: Any other appropriate method for derivation can be considered.	Definition α and β-1M each Derivation-2M

	(b)	**Explain need of biasing. List any two methods of biasing.**	**4M**
	Ans:	**Need of Biasing:** The need of biasing is to obtain a certain dc collector current at a certain dc collector voltage. That is for selection of operating point. The biasing arrangement Methods of biasing: 1. Fixed bias. 2. Collector-to-base bias. 3. Fixed bias with emitter resistor. 4. Voltage divider bias or potential divider. 5. Emitter bias.	**Need of biasing-2M** **Any two method-2M**
	(c)	**With the help of diagram, explain the working of N-channel JFET.**	**4M**
	Ans:	 Working:	**Diagram -2M** **Working -2M**

1. The application of negative gate voltage or positive drain voltage with respect to source, reverse biases the gate- source junction of an N-channel JFET. The effect of reverse bias voltage is to form depletion regions within the channel.

2. When a voltage is applied between the drain & source with dc supply voltage (V_{DD}), the electrons flows from source to drain through the narrow channel existing between the depletion regions. This constitutes the drain current (I_D)& its conventional direction is from drain to source. The value of drain current is maximum, when no external voltage is applied between the gate & source & is designated by the symbol IDSS.

3. When V_{GG} is increased, the reverse bias voltage across gate-source junction is increased. As a result of this depletion regions are widened. This reduces the effective width of the channel & therefore controls the flow of drain current through the channel.

4. When gate to source voltage (V_{GG}) is increased further, a stage is reached at which both depletion regions touch each other as shown in fig (b).

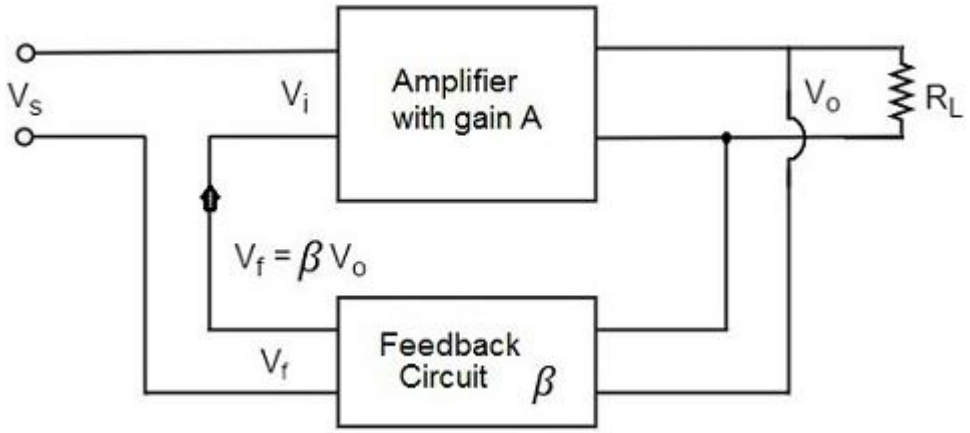
5. At this value of V_{GG}, channel is completely blocked or pinched off & drain current is reduced to zero. The value of V_{GS} at which drain current becomes zero is called pinch off voltage designated by the symbol V_P or V_GS(OFF) . The value of V_P is negative for N-channel JFET.

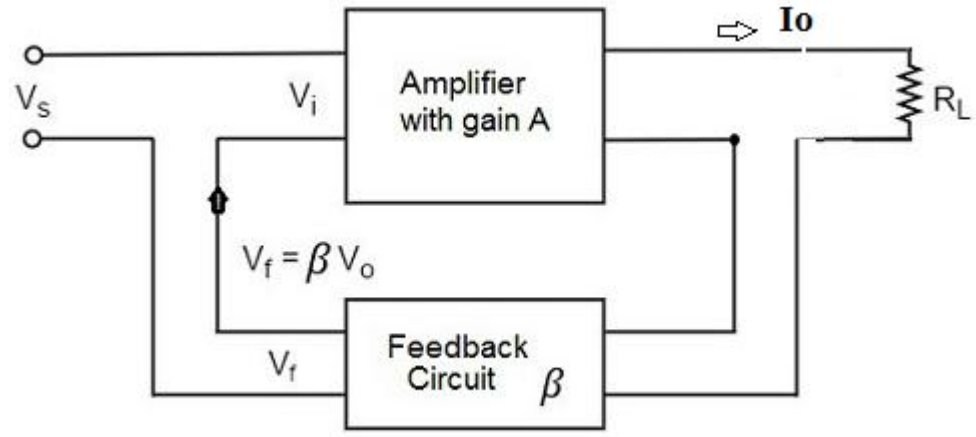
(d) Compare CB, CC, CE configuration(any 4 points). **4M**

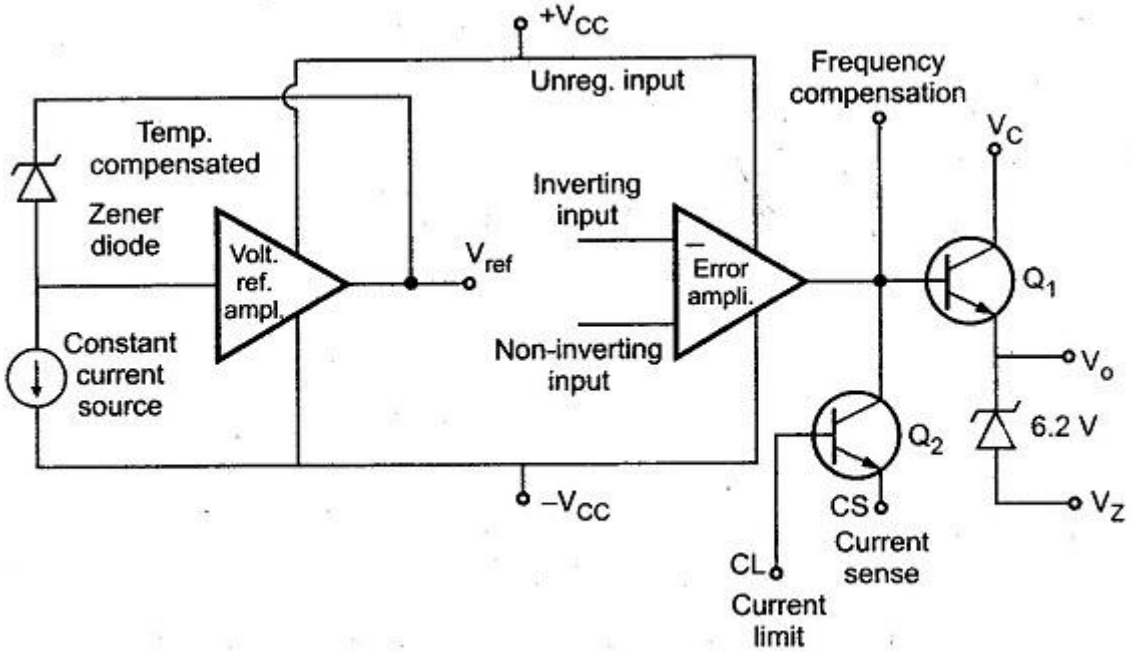
Ans:

Characteristic	Common base (CB)	Common collector,(CC)	Common emitter,(CE)
Input Dynamic Resistance	Very Low(less than 100 ohm)	Very High(750K)	Low(less than 1K)
Output Dynamic Resistance	Very High	Low	High
Current Gain	Less than 1	Very High	High

Any four points- 1M each

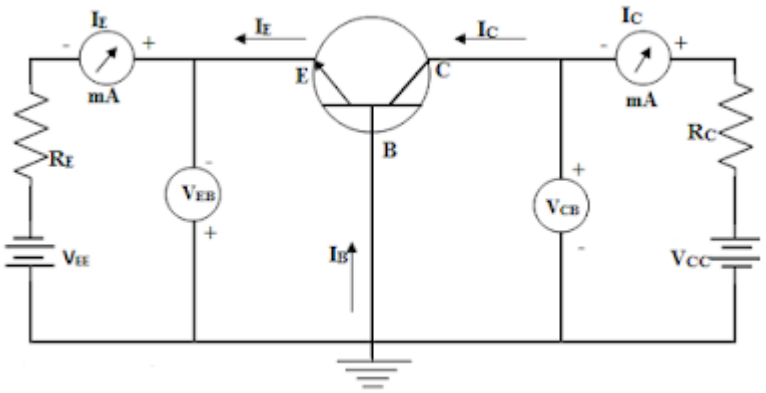
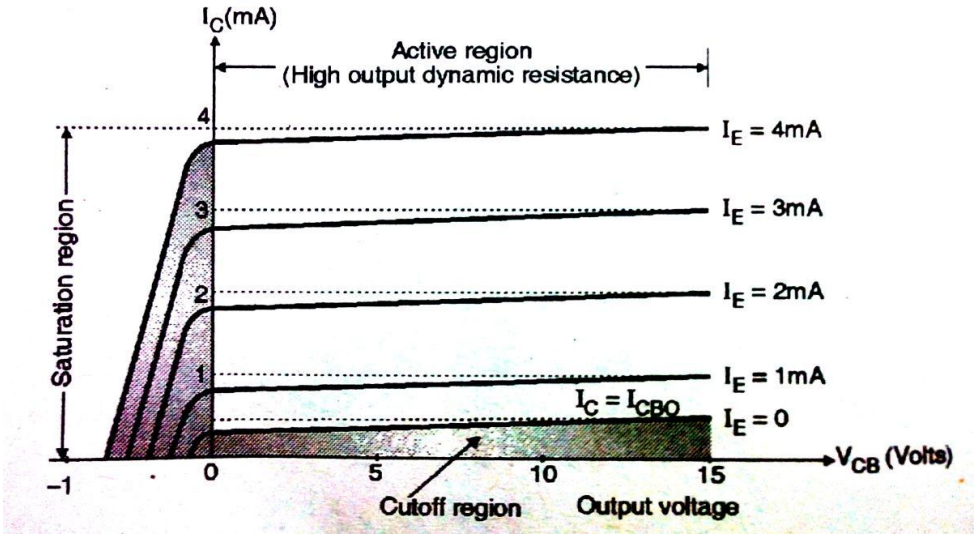
			Voltage gain	Greater than CC but less than CE	Lowest(less than 1)	Highest	
			Power gain	Medium	Medium	Highest	
			Leakage current	Very small	Very large	Very large	
			Relationship between I/p and o/p	In phase	In phase	Out of phase(180º)	
			Application	For High freq. applications	For impedance Matching Applications	For Audio freq. Applications	
	(e)	**Draw block diagram of voltage series and current series feedback.**					**4M**
	Ans:	**Block diagram of Voltage series feedback:**  Block Diagram of Current Series:					**2M each Diagram**

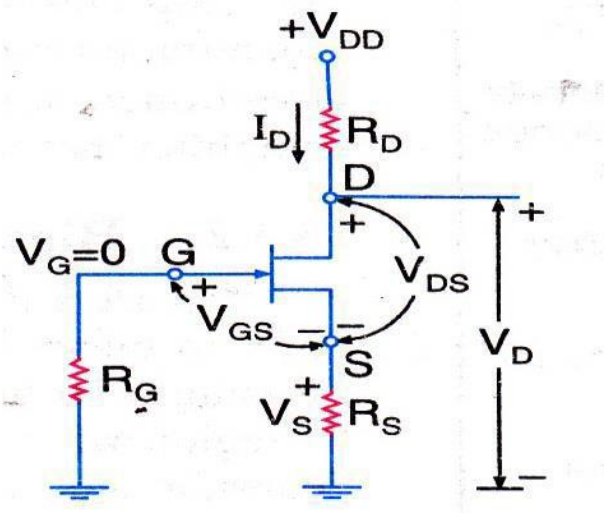


	(f)	**Draw the functional block diagram of IC 723. Describe it's working.**	**4M**
	Ans:	**Functional Block Diagram:**  The functional diagram of the voltage regulator is shown below. It consists of a voltage	**Functional block diagram -2M** **Working -2M**

		reference source, an error amplifier, a series pass transistor and a current limiting transistor. The device can provide voltage with an output voltage ranging from 2 V to 37 V, and output current levels up to 150 m A. The working can be explained by dividing it into two blocks, **the reference voltage generator** and **the error amplifier**. In the reference voltage generator, a Zener diode is being compelled to operate at fixed point (so that zener output voltage is a fixed voltage) by a constant current Source which comes along with an amplifier to generate a constant voltage of 7.15V at the Vref pin of the IC. As for the error amplifier section, it consists of an error amplifier, a series pass transistor Q1 and a current limiting transistor. The error amplifier can be used to compare the output voltage applied at Inverting input terminal through a feedback to the reference voltage Vref applied at the Non-Inverting input terminal. This connection is not provided internally and so has to be externally provided in accordance with the required output voltage. The conduction of the transistor Q1 is controlled by the error signal. It is this transistor that controls the output voltage	

Q. No.	Sub Q. N.	Answers	Marking Scheme
3		**Attempt any FOUR :**	**16- Total Marks**
	(a)	**Draw the circuit diagram for common base configuration and draw its output characteristics.**	**4M**

	Ans:	 	Circuit Diagram : 2M Output Characteristics: 2M
	(b)	Describe source self bias method of FET with neat circuit diagram.	4M

	Ans:	 **Explanation:** Fig shows the circuit of source biasing for JFET. • FET gate is grounded through resistor R_G. • Source is grounded through resistor R_s. • Only one Drain supply V_{DD} is required. • Drain current I_D flows when Drain voltage is applied. • This Drain current produces a voltage drop across R_S. This provides the reverse voltage at Gate for FET operation. **D.C. analysis:-** From the circuit:- For V_{GS} apply KVL as shown – $-V_{GS} – V_S = 0$ $-V_{GS} - I_D.R_S = 0$ since $I_D = I_S$ $V_{GS} = - I_D.R_S$ Expression for VDS,	**Circuit Diagram : 2M** **Working : 2M**

Apply KVL to the drain circuit

$V_{DD} - I_D R_D - V_{DS} - I_S R_S = 0$

$V_{DD} = I_D (R_D + R_S) + V_{DS}$ since $I_D = I_S$

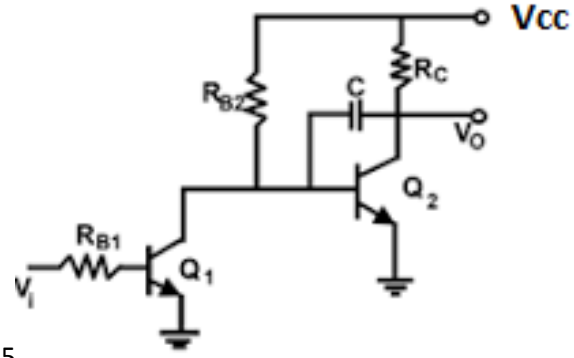
$V_{DS} = V_{DD} - I_D (R_D + R_S)$

The value of the drain current can be obtained by Shockley's equation. Thus the Q point of JFET amplifier using source biasing is given by,

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{DS(off)}}\right)^2$$

(c) **Draw miller sweep generator and give its two applications.** **4M**

Ans:



45 S

Circuit Diagram : 1M

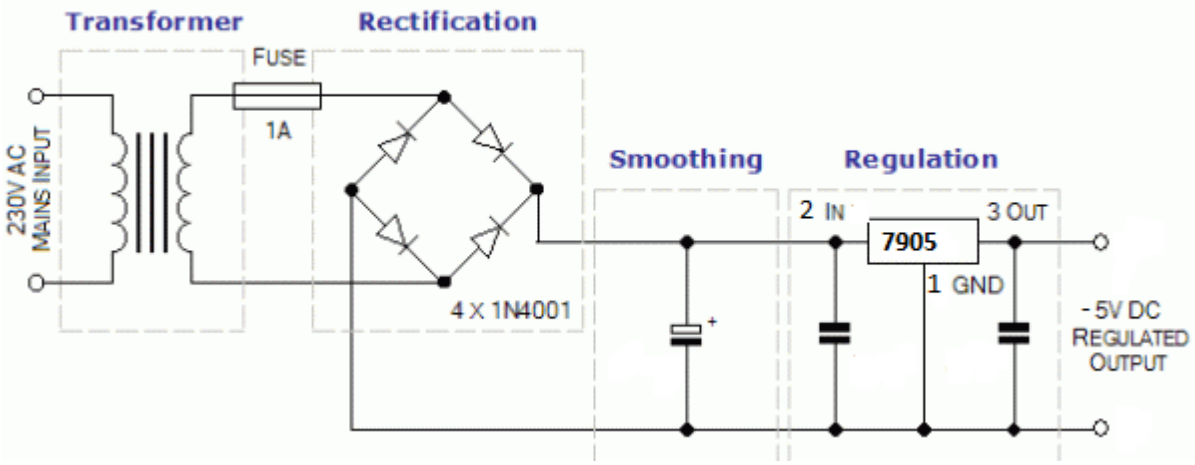
Applications:2M

Applications of miller sweep:

1. Applications where linear output is expected.
2. In Television (TV)
3. In CRO
4. To convert step waveform into ramp waveform.

(d)	**Compare the different types of coupling (any 4 points).**		**4M**
Ans:			**Any 4 points: 1M each**

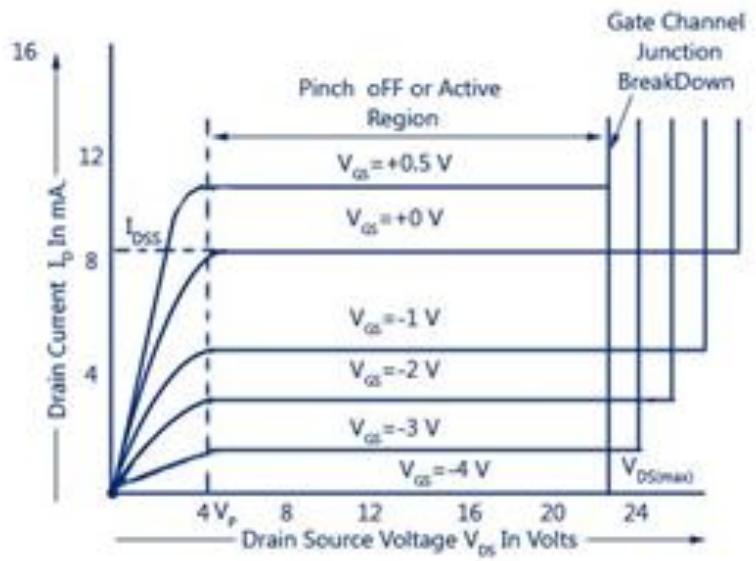
Parameters	**RC Coupled**	**Transformer coupled**	**Direct coupled**
Frequency response	Excellent in audio frequency range	Poor	Best
Cost	Less	More	Least
Space and weight	Less	More	Least
Impedance matching	Not good	Excellent	Good
Applications	For voltage amplification	For power amplification	For amplifying low frequency signals
Type of coupling	Resistor- Capacitor	Transformers	No coupling

(e)	**Draw the circuit diagram of -5 V regulator using 7905 and describe its working.**		**4M**
Ans:			**Circuit Diagram : 2M** **Working: 2M**

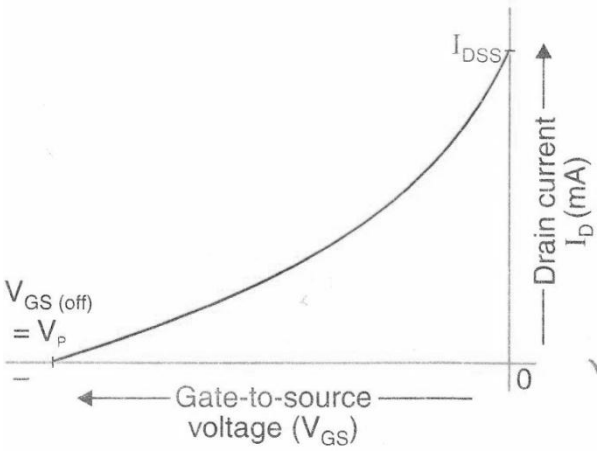
- The AC signal is given through an input transformer which steps up or down according to the usage. Mostly a step down transformer is used in rectifier circuits, so

		as to reduce the input voltage. • Rectifier used is a full wave rectifier which converts AC input into pulsating DC output. • Capacitors are the filter capacitors. It is used to reduce noise or oscillations from unregulated input as well as it improves the transient response. • IC 7905 is a 3 pin regulator IC which is used to produce a regulated -5V output.	
	(f)	**Define the following: (1) Load Regulation (2) Line Regulation.**	**4M**
	Ans:	**(i) Load Regulation** The load regulation indicates the change in output voltage that will occur per unit change in load current. Mathematically, $\% L.R = \frac{V_{NL}-V_{FL}}{V_{FL}} * 100$ where, V_{NL}= Load voltage with no load current V_{FL}= Load voltage with full load current **(ii) Line Regulation** The line regulation or source regulation rating of a voltage regulator indicates the change in output voltage that will occur per unit change in the input voltage. Mathematically, $\% S.R = \frac{V_{HL}-V_{LL}}{V_N} * 100$ where,	**Definition :** **2M each**

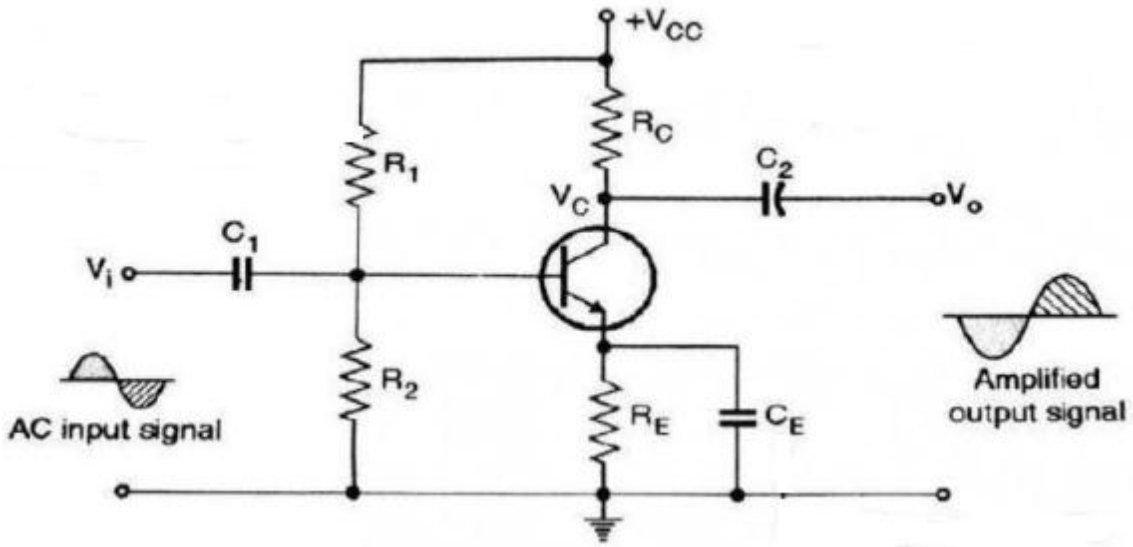
		V_{HL}= Load voltage with high line voltage V_{LL}= Load voltage with low load current V_N = output voltage under normal operating conditions	
Q. No.	Sub Q. N.	Answers	Marking Scheme
4		**Attempt any FOUR :**	**16- Total Marks**
	(a)	**List 4 applications of FET. Draw the drain and transfer characteristics of JFET.**	**4M**
	Ans:	**Applications of FET:** **1.** Used as a buffer amplifier. **2.** Used as an electronic switch. **3.** Used in radio frequency amplifiers for FM devices **4.** Used in low frequency amplifiers due to its small coupling capacitors. **5.** Used in **large scale integration** (LSI) and computer memories because of its small size. **6.** Used in mixer circuits to control low inter modulation distortions. **Drain characteristics of JFET**	**Applications (any 4 points) : 2M** **Drain characteristics : 1M** **Transfer characteristics : 1M**

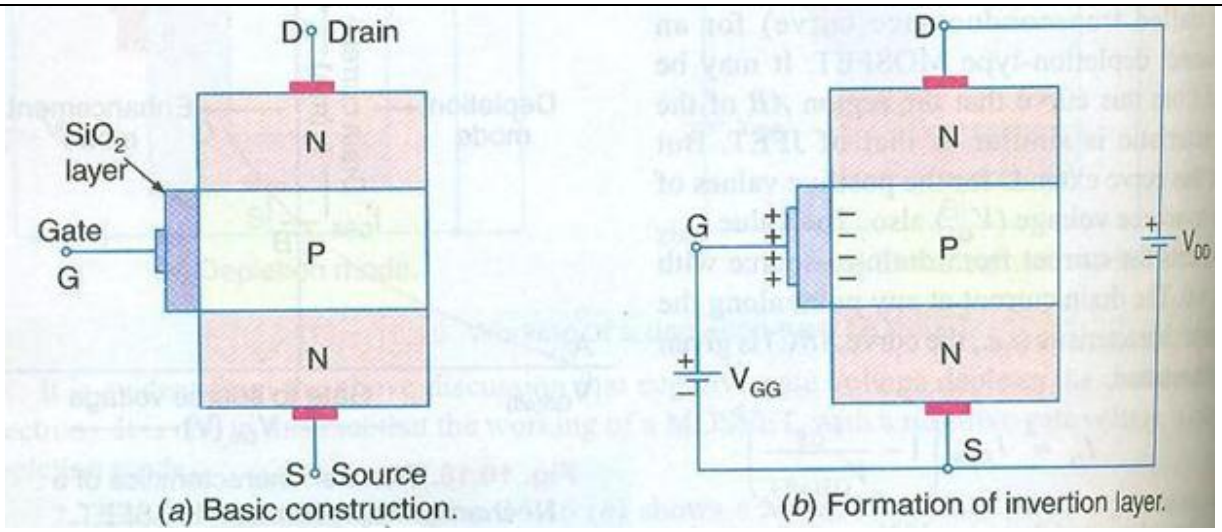


Transfer characteristics of JFET:

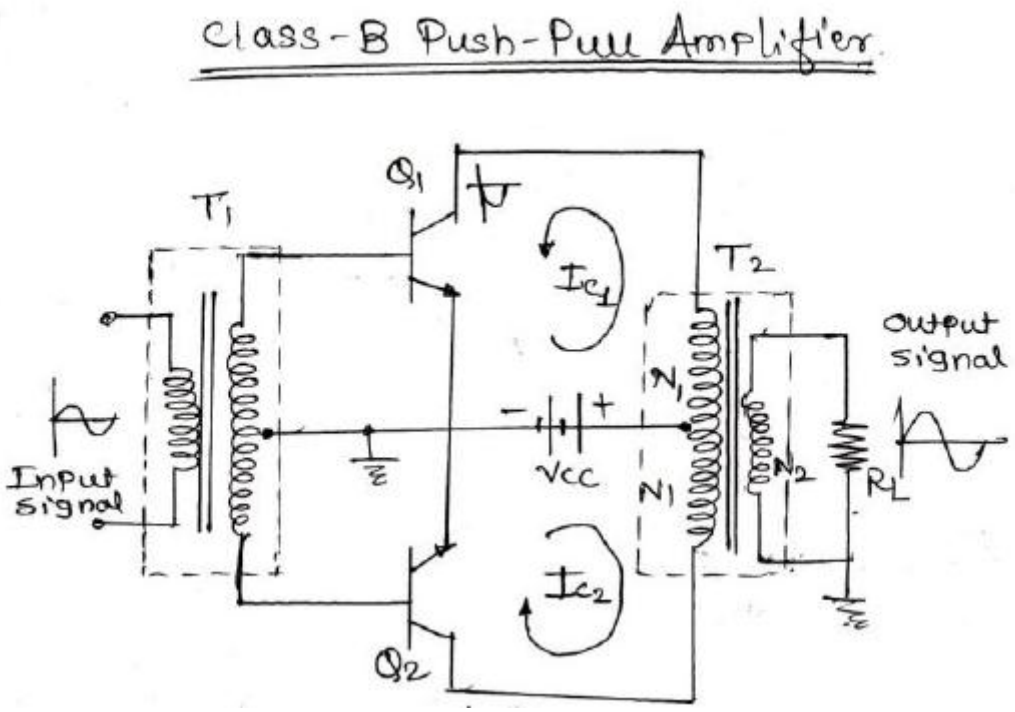


	(b)	**Draw the diagram of single stage CE amplifier and state the function of each component.**	**4M**

	Ans:	 **Function of Components:** 1. Biasing circuit: Resistors R1, R2 and RE form biasing and stabilization circuit. It establishes a proper operating point. 2. Input Coupling Capacitor C1: Used to couple the input AC signal to base of transistor. It allows only AC signal to flow but opposes DC. 3. Output Coupling Capacitor C2: Used to connect the transistor amplifier to the next stage. It allows only AC signal to flow but opposes DC. 4. Emitter bypass capacitor: It provides a low reactance path to the amplified signal. It bypasses all the currents from the emitter to the ground.	**Circuit Diagram : 2M** **Functions : 2M**
	(c)	**Describe the construction, operation of E-MOSFET.**	**4M**

	Ans:	 The enhancement type MOSFET has no depletion mode and it operates only in enhancement mode. It differs in construction from the depletion type MOSFET in the sense that it has no physical channel. It may be noted that the P- type substrate extends the silicon dioxide layer completely. This MOSFET is always operated with the positive gate to source voltage. When the gate to source voltage is zero. The V_{DD} supply tries to force free electrons from source to drain but the presence of P- region does not permit the electrons to pass through it. Thus there is no drain current for VGS= 0. Due to this fact, the enhancement type MOSFET is also called normally OFF MOSFET. Now if some positive voltage is applied at the gate, it induces a negative charge in the P-type substrate just adjacent to the silicon dioxide layer. The induced negative charge is produced by attracting the free electrons from the source. When the gate is positive enough, it can attract a number of free electrons. This form a thin layer of electrons, which stretches from source to drain, This effect is equivalent to producing a thin layer of N- type channel in	**Construction: 2M;** **Operation: 2M**

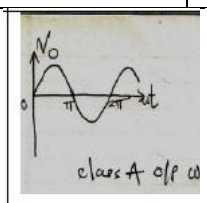
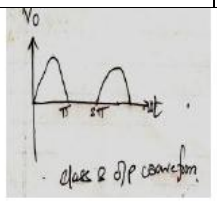
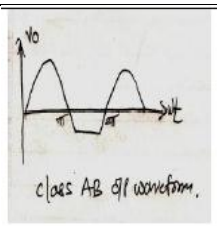
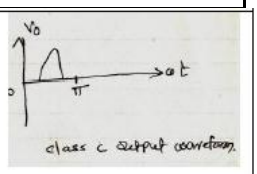
		the P- type substrate. This layer of free electrons is called N- type inversion layer. The minimum gate to source voltage which produces inversion layer, is called threshold voltage V_{GST}. When the voltage V_{GS} is less than V_{GST} no current flows from drain to source. However when the voltage V_{GS} is greater than V_{GST} the inversion layer connects the drain and source and we get significant value of current.	
	(d)	**Describe class B push pull amplifier with neat circuit diagram.**	**4M**
	Ans:	• In class B amplifier transistor conducts only for half cycle of input signal. This type of output signal gives large distortion. In order to avoid this we use two transistors connected in push-pull arrangement. One conducts in positive half cycle and other conducts in negative half cycle. • Transistor T1 is called as input transformer and is called phase splitter and produces two signals which are 180º out of phase with each other. Transistor T2 is called output transformer and is required to couple the a.c. output signal from the collector to the load.	**Circuit Diagram : 2M** **Explanation : 2M**



Working:

- When there is no input signal both the transistor Q1 and Q2 are cut-off. Hence no current is drawn from VCC supply. Thus in standby the power dissipation in both transistor is practically zero and there is no power wasted.
- During positive half cycle the base of Q1 is positive and Q2 is negative. As a result of this Q1 conducts, while the transistor Q2 is OFF. And a half cycle is obtained at the output.
- During negative half cycle, Q1 turns OFF and Q2 conducts, and another half cycle is obtained at the output. At any instant only one transistor in the circuit is conducting. Each transistor handles one half of the input signal.
- Then output transformer joins these two halves and produces a full-sine wave across the load resistor.

	(e)	**Compare class A, class B and class C power amplifier on (1) position of operating point (2) efficiency (3) conduction angle (4) O/P waveform.**	**4M**
	Ans:		**4 points : 4M**

Parameters	**Class A**	**Class B**	**Class AB**	**Class C**
1) Position of operating point	At the centre of the load line	On X axis	Above X axis and below centre of the load line	Below X axis
(2) Efficiency	Maximum 50%	Maximum 78.5%	Between Class A & Class B	Very high, can be almost 100%
(3) Conduction angle	Conducts for full cycle (360^0) of input cycle	Conducts for half cycle (180^0) of input cycle	Conducts for more than half cycle and less than full cycle of input cycle	Conducts for less than half cycle of input cycle
(4) O/P waveform.				

	(f)	**What is oscillator? State applications of oscillator.**	**4M**
	Ans:	**Oscillator:**	**Definition : 1M**

		Oscillator is basically an ac signal generator which generates alternating voltage of desired shape at desired frequency. Oscillators work on the principle of positive feedback. **Applications of oscillator** 1. In the radio and TV transmitters. 2. In Special type receivers. 3. As a crystal clock in microprocessors. 4. In the frequency synthesizers.	**Applications (any 3 points) : 3M**
Q. No.	Sub Q. N.	Answers	Marking Scheme
5.		**Attempt any FOUR :**	**16- Total Marks**
	(a)	**In C.E. configuration if β = 150, leakage current ICEO = 100 μA and base current is 0.5 mA, determine I_C and I_E.**	**4M**

	Ans:	5a) Given data : $\beta = 150$ $I_{CEO} = 100\mu A$ $I_B = 0.5\,mA$ $I_C = ?$ $I_E = ?$ $I_C = \beta \cdot I_B + I_{CEO}$ $= 150 \times 0.5 \times 10^{-3} + 150 \times 10^{-6}$ $= 75 \times 10^{-3} + 0.1 \times 10^{-3}$ $\therefore I_C = 75.1\,mA$ $\because I_E = I_C + I_B$ $= 75.1 + 0.5$ $\therefore I_E = 75.6\,mA$	**1 mark** **1mark** **1 mark** **1 mark**
	(b)	**State the advantages and disadvantages of crystal oscillator.**	**4M**
	Ans:	**Advantage of crystal oscillator** 1)It provides high degree of stability 2) It provides high degree of accuracy. 3) The Q is very high. 4) It is Possible to obtain very high, Precise and stable frequency of oscillations. 5) Very low frequency drift due to change in temperature and other parameters. **Disadvantage of crystal oscillator** 1) It is suitable for only low power circuit. 2) Different frequency cannot be obtained easily.	**2marks(any two)** **2marks(any two)**

3) Very high frequency can't be produced

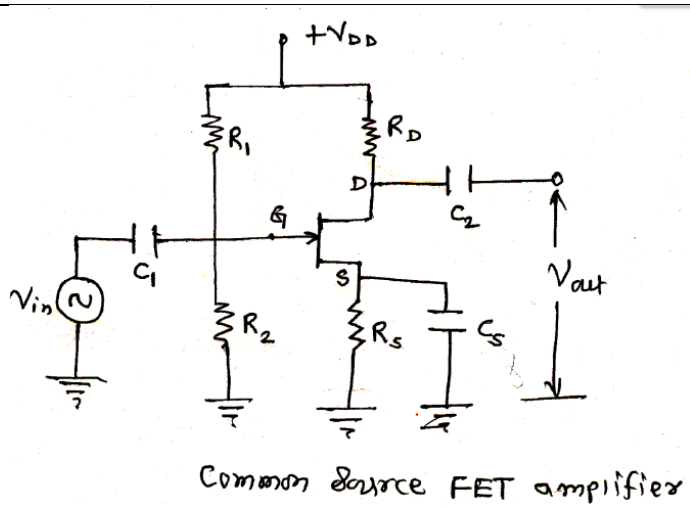
4) Less range of frequencies can be obtained.

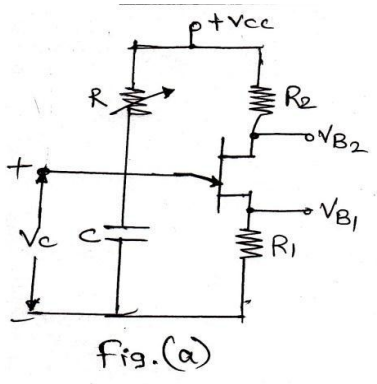
(c) Compare small signal amplifier (voltage amplifier) and power amplifier. **4M**

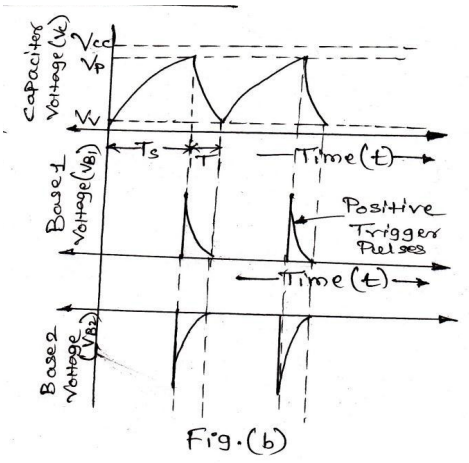
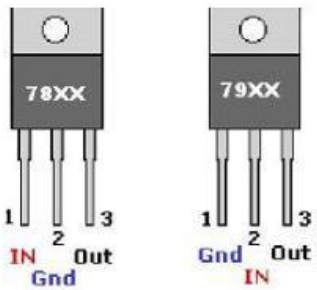
Ans:

Sr.No.	Small Signal Amplifier/ voltage amplifier	Power Amplifier
1	Transistor used in voltage amplifier has a large value of current gain (β) is nearly 100 as compare to that of power amplifier.	Transistor used in power amplifier has current between 20& 50
2	The input voltage to base of transistor in voltage amplifier is low (a Few mV).	The input voltage to base of transistor in power amplifier is high (2-4 V)
3	Input resistance is quite low as compare to output resistance.	Input resistance is very large as compared to output resistance
4	The physical size of the transistor used in voltage amplifier is used in voltage small known as low or medium power transistor.	Power amplifier uses larger size transistors.
5	Voltage amplifier uses RC coupling for interstate	Power amplifier uses transformer coupling.

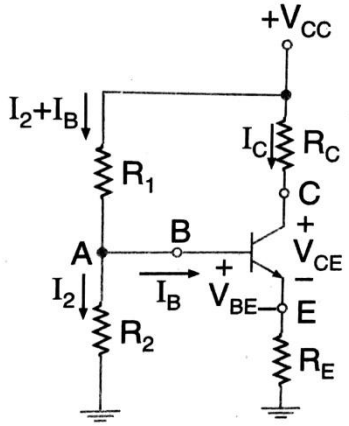
4 marks for any four points

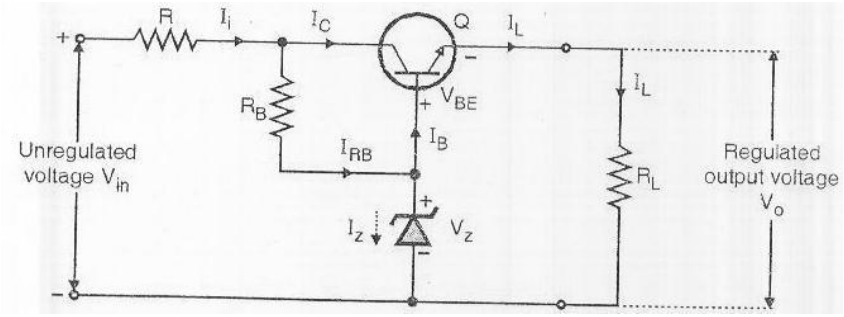
				connection.		
			6	The a.c. power output is low	The a.c. power output is high	
			7	The amplitude of input a.c. signal is small	The amplitude of input a.c. signal is large	
			8	The collector current is low about 1mA	The collector current is very high usually greater than 100 mA	
	(d)	**Draw common source FET amplifier. Describe its operation.**				**4M**
	Ans:	 Common Source FET amplifier **Operation:** - When small a.c. signal is applied to the gate, it produces variation in the gate to source voltage. This produces variation in the drain current. As the gate to source voltage increases, the drain current also increases. As the result of this voltage drop across R_D also increases. This causes the drain voltage to decreases. In positive half cycle of the input ac signal: As the input voltage rises, gate to source voltage becomes less negative, it will increase the channel width and increase the level of drain current I_D. As the input voltage falls, it will decrease the channel width and decrease the level of drain current I_D.				**2 marks for diagram** **2 marks for operation**

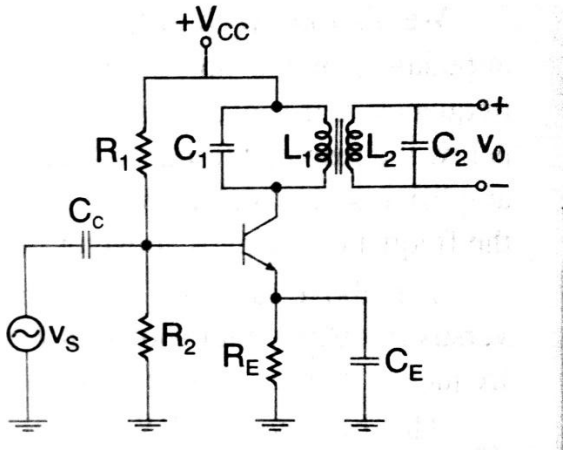
		Thus I_D varies sinusoidally above its Q point value. The drain to source voltage V_{DS} is given by $V_{DS} = V_{DD} – I_DR_D$. Therefore as I_D increases the voltagedrop I_DR_D will also increase and voltage V_{DS} will decrease. If ΔI_D is large for a small value of ΔV_{GS} , the ΔV_{DS} will also be large and we get amplification. Thus the AC output voltage V_{DS} is 180º out of phase with AC input voltage.	
	(e)	**Describe the working principle of UJT as relaxation oscillator with neat circuit diagram.**	**4M**
	Ans:	**Circuit Diagram:**  fig.(a)	**2 marks for diagram**
		Circuit Operation: When the supply voltage V_{CC} is switched ON, the capacitor C charges through resistor R, till the capacitor voltage reaches the voltage level V_P which is called as peak point voltage. At this voltage, the UJT turns ON; and capacitor C discharges rapidly through resistor R_1. When the capacitor voltage drops to Vv level (called valley-point voltage) the UJT switches OFF, allowing capacitor C to charge again. Because of charging and discharging of capacitor saw tooth waveforms are obtained at emitter terminal and positive trigger pulse is obtained at Base 1 and negative trigger pulses	**2 marks for working**

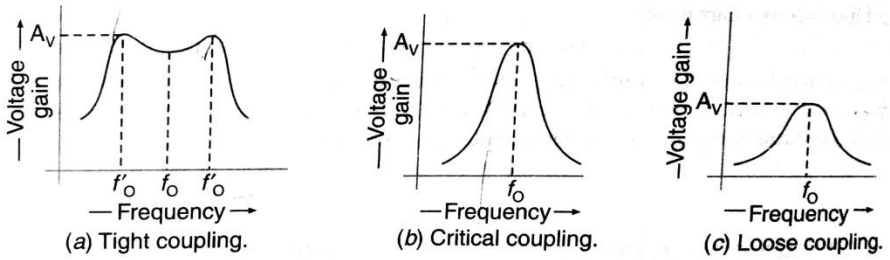
		are obtained at base 2 as shown in Fig. (b) The sweep period is given by the relation, $T = R.C. \log_e (1/1-n)$ $T = 2/3\ R.C. \log_{10}(1/1-n)$ Where, η is intrinsic stand-off ratio The sweep frequency can be varied by changing values of either R or C.  Fig. (b)	
	(f)	**Draw pin diagram of IC 78XX and IC 79XX and state their features and advantages.**	**4M**
	Ans:	 **Features: (Any Two)**	**2 marks** **(Each pin 1 mark)** **1 mark for two**

		1. Programmable output. 2. Facility to boost the voltage/current. 3. Internally provided short circuit current limiting. 4. Thermal Shutdown. 5. Floating operation to facilitate higher voltage output. 6. Versatility and low cost. 7. They are easy to use. **Advantages: (Any One)** 1. 78xx and 79xx series ICs do not require additional components to provide a constant, regulated source of power, making them easy to use, as well as economical and efficient uses of space. 2. 78xx and 79xx series ICs have built-in protection against a circuit drawing too much current. They have protection against overheating and short-circuits, making them quite robust in most applications.	**features** **1 mark for advantage**
Q. No.	Sub Q. N.	Answers	Marking Scheme
6.		**Attempt any FOUR :**	**16- Total Marks**
	(a)	**Explain with a neat circuit, voltage divider bias method for biasing a transistor.**	**4M**

	Ans:	 **Voltage divider bias circuit** Explanation:- The name voltage divider is derived from the fact that resistor R_1 and R_2 form a potential divider across the V_{CC} supply. The voltage drop across resistor R_2 forward biases the base – emitter junction of a transistor. The emitter resistor (R_E) provides the D.C. stability. It is evident from the circuit that due to the voltage divider network of resistors R_1 and R_2, the voltage at the transistor base is $V_B=Vcc*R_2/(R_2+R_1)$ (considering V_{BE} negligibly small) Therefore value of emitter current, $I_E = V_E/R_E$ And the value of collector current, $I_C = I_E$ (approximately) The voltage drop across the collector resistor, $V_{RC} = I_C * R_C$ And the voltage at the collector (measured with respect to the ground) $V_C = V_{CC} - V_{RC} = V_{CC} – I_C * R_C$	**2 marks for circuit** **2 marks for explanation**

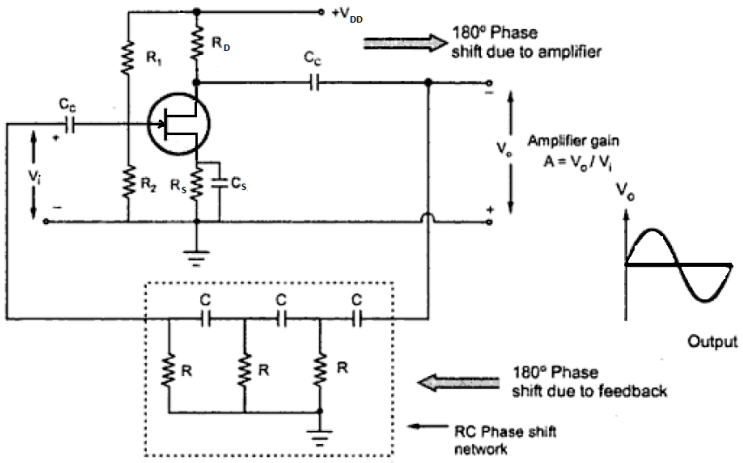
		The voltage from collector – to – emitter. $V_{CE} = V_C - V_E = V_{CC} - I_C * R_E$ $V_{CE} = V_{CC} - I_E(R_C + R_E)$ ……(I_C = I_E)	
	(b)	**Draw the circuit of series transistor voltage regulator and describe its operation.**	**4M**
	Ans:	 **Explanation :** • In this circuit transistor Q acts as a control element. This transistor Q is connected in series with the load R_L, hence the circuit is called as Series Voltage Regulator. Other components in the circuit are Zener diode (V_Z), and two resistors R & R_B. • Zener diode V_Z is operated in breakdown region and provides constant voltage V_Z. • Resistance R_B provides the limiting current to Zener diode. • The total current in the circuit is decided by resistance R. • As V_Z& V_{BE} of the transistor are constant, output voltage across R_L will also be constant. To find output voltage V_O, Applying KVL to o/p loop of the circuit $V_{BE} + I_L R_L - V_Z = 0$ Therefore, $V_O = I_L R_L = V_Z - V_{BE}$ **$V_O = V_Z - V_{BE}$** As V_{BE} is constant and negligibly small (approx. 0.6V to 0.7V). Therefore output voltage of this circuit is decided by Zener diode V_Z.	**2 marks for circuit** **2 marks for explanation**

	(c)	**State the meaning of positive and negative feedback**	**4M**
	Ans:	**Positive feedback:** If the feedback signal (voltage or current) is applied in such a way that it is in phase with the input signal and thus increases it, then it is called a positive feedback. It is also known as regenerative feedback or direct feedback. **Negative feedback**: If the feedback signal (voltage or current) is applied in such a way that it is out phase with the input signal and thus decreases it, then it is called a negative feedback. It is also known as degenerative feedback or inverse feedback.	**2 marks** **2 marks**
	(d)	**Draw the circuit of double tuned amplifier and sketch the frequency response.**	**4M**
	Ans:	**Double tuned amplifier:-**  **Frequency response:-**	**2 marks for circuit** **2 marks for respons e**



(e) **Draw circuit of RC phase shift oscillator and describe its working.** **4M**

Ans:



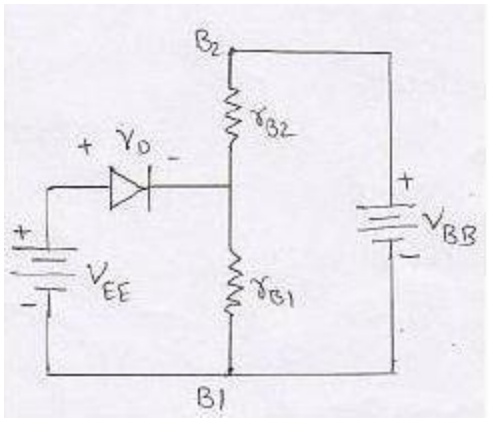
2 Marks for diagram

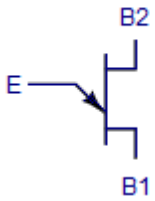
(Note:Diagram with transistor is also accepted)

Working: The circuit is drawn to show clearly the amplifier and feedback network. The amplifier stage is self-baised with a capacitor by-passed source resistor (R_s) and drain bias resistor(R_D) .

2 Marks for working

The feedback network consists of three identical RC sections. Each section produces a phase shift of 60^0. Therefore the net phase shift of the feedback network is 180^0. Since the amplifier stage also introduces a phase shift of 180^0, therefore total phase shift between the input and output circuit is 360^0 or 0^0.

		When the circuit is energized, by switching on the supply, the circuit starts oscillating. The oscillations may start due to the minor variation in D.C. supply or the inherent noise in the FET. The variation in the gate current is amplified in the drain circuit. Then it is fedback through the phase shift network and finally applied to the gate. The circuit frequency of oscillation is given by the relation, $f_{ob}=\frac{1}{2\pi RC\sqrt{6}}$	
	(f)	**Explain the construction of UJT and draw its symbol.**	**4M**
	Ans:	 Fig. shows the equivalent circuit of a unijunction transistor with voltage source V_{EE} connected across emitter and base1 and V_{BB} connected across base1 and base2. Hence the diode is reversed biased by a voltage drop across the r_{B1} and its own barrier potential (V_D). Thus total reverse bias voltage across a diode is equal to sum of $\eta.V_{BB}$ and V_D. As long as the V_{EE} is below the total reverse bias voltage (i.e. $\eta.V_{BB} + V_D$) across the diode, it remains reverse biased and there is no emitter current. However if the V_{EE} voltage reaches or exceeds the value equal to ($\eta.V_{BB} + V_D$), the diode conducts V_{EE}, which causes the diode to conduct, is called peak point voltage.	**1 Marks for diagram** **2 Marks for Explanation**

		$V_P = \eta . V_{BB} + V_D$ When the emitter current begins to flow, the UJT is said to be fired, triggered or turned on. **Symbol of UJT:**  	**1 Marks for symbol**