WINTER– 18 EXAMINATION

Subject Name: Principles of Digital Techniques **Model Answer** Subject Code: 17320

Important Instructions to examiners:

1) The answers should be examined by key words and not as word-to-word as given in the model answer scheme.
2) The model answer and the answer written by candidate may vary but the examiner may try to assess the understanding level of the candidate.
3) The language errors such as grammatical, spelling errors should not be given more Importance (Not applicable for subject English and Communication Skills.
4) While assessing figures, examiner may give credit for principal components indicated in the figure. The figures drawn by candidate and model answer may vary. The examiner may give credit for any equivalent figure drawn.
5) Credits may be given step wise for numerical problems. In some cases, the assumed constant values may vary and there may be some difference in the candidate's answers and model answer.
6) In case of some questions credit may be given by judgement on part of examiner of relevant answer based on candidate's understanding.
7) For programming language papers, credit may be given to any other program based on equivalent concept.

1 a) Attempt any six of the following: **Marks 12**

(i) Represent the decimal no. 27 in binary form using BCD code and Gray code.

Ans: (correct BCD code: 1M; correct Gray code: 1M)

$(27)_{10} = \quad (\ )_2$

2	27	
2	13	1 (LSB)
2	6	1
2	3	0
	1	1
		1 (MSB

$= (11011)_2$

BCD code of $(27)_{10}$ =$(0010\ \ 0111)_2$

Gray code of $(27)_{10}$ =

1	1	0	1	1
↓	↓	↓	↓	↓
1	0	1	1	0

$(27)_{10}$ =$(10110)_{Gray}$

(ii) Draw the logic diagram of half subtractor and write its truth table.

Ans :(logic diagram 1M,truth table 1M)

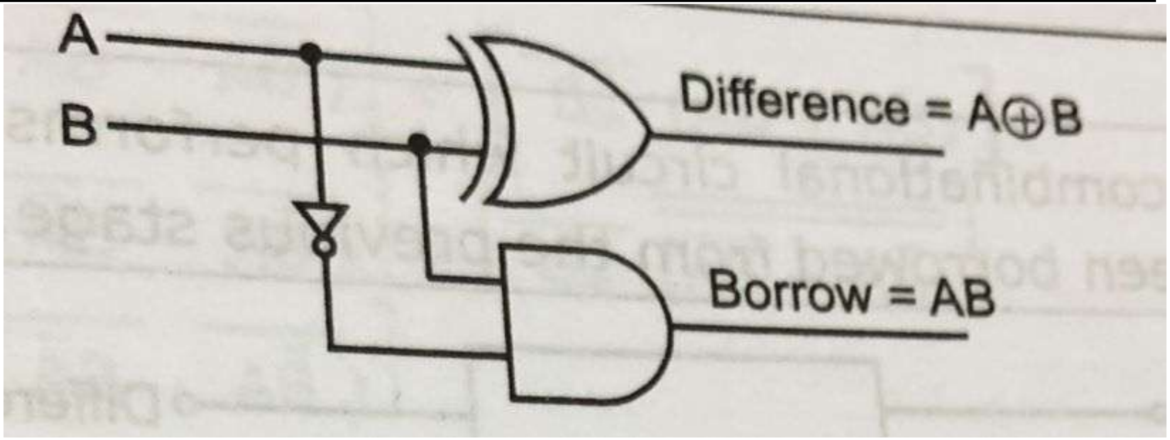


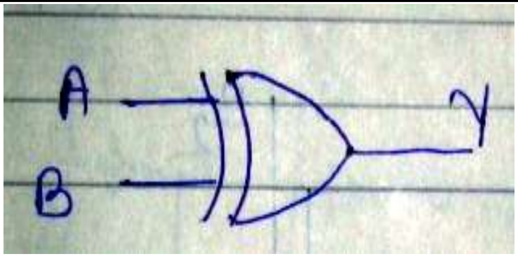
Fig: logic diagram of half subtractor

Truth table of half subtractor:

Inputs		**Outputs**	
A	**B**	**Difference D**	**Borrow**
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

(iii) Draw the symbol of EX-OR gate along with truth table.

Ans : (symbol 1M, truth table 1M)



Logical equation = A XOR B OR

$= A\bar{B} + \bar{A}B$

Truth table

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

(iv) What is meant by modulus of a counter?
Ans : (correct definition 2M)

The total number of discrete states through which a counter can pass is called as modulus of a counter.

A counter consisting of a flip flop can count $N=2^n$ discrete states.

(v) Define the following specifications of DAC. (1) Resolution (2) Linearity.

Ans :(each definition 1M)

Resolution: The smallest possible change in the analog output that is affected by a unit change in digital input is known as resolution of a D/A converter.

Linearity: The Linearity of a D/A converter is a measure of the precision with which the linear input-output relationship is satisfied.

(vi) Compare EPROM and flash memory.(any two points)

Ans : (each comparison 1M)

Sr No.	EPROM	FLASH
1	Can be erased only byte by byte by giving electrical pulse	Can be erased block by block by giving electrical pulse
2	Byte programmable	Block programmable
3	Cost is more	Cost is less
4	Programming is faster	Programming is faster

(vii) Draw the logical diagram of bit memory cell using NAND gates only.

Ans : (correct logical diagram 2M)

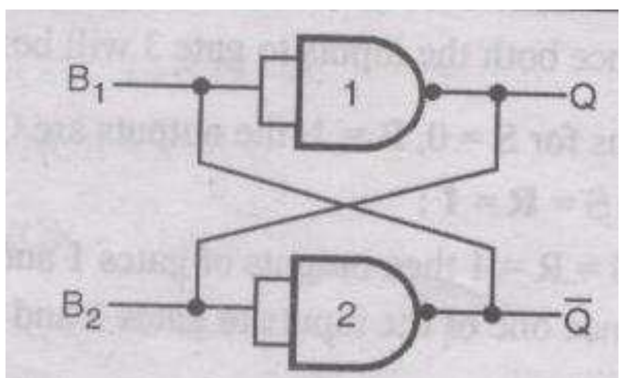


Fig: bit memory cell using NAND gates only

(viii) List the types of ADC's and DAC's:

Ans : (list of ADC's 1M ,list of DAC's 1M)

Various types of ADC's are:

1. Ramp type ADC
2. Single slope ADC
3. Dual slope ADC
4. Successive Approximation type ADC

Types of DAC's are:

1. Binary Weighted Resistor
2. R-2R Ladder type DAC

b) Attempt any Two of the following: Marks 8

(i) Perform the binary subtraction using 1's and 2's complement method.

i) $(52)_{10} - (65)_{10}$

Ans: (each correct answer: 2M)

$(52)_{10} - (65)_{10}$

$(52)_{10} = (00110100)_2$

$(65)_{10} = (01000001)_2$

1's complement subtraction

```
    52              00110100
-   65            + 10111110
______          ____________
   -13              11110010
```

As carry is not generated answer is –ve & in 1's complement form

Therefore 1's complement of answer is $-(00001101)_2$

$= (-13)_{10}$

2's complement subtraction

52 2's complement of 65 $\Leftrightarrow$11111)

```
-   65
______
-   13
        00110100
      + 10111111
      __________
        11110011
```

As carry is not generated answer is –ve & its 2's complement form

Therefore 2's complement of result is $-(00001101)_2$

$= -(1101)_2$

$= -(13)$

ii) **Define priority encoder. Draw the truth table of decimal to BCD encoder**.

Ans : (definition 2M,truth table 2M)

A logic circuit that responds to just one input in accordance with some priority system , among all those that may be simultaneously high is called a priority encoder.

Truth table of decimal to BCD encoder is as follows:

Active low decimal inputs									Active low BCD outputs			
1	2	3	4	5	6	7	8	9	D	C	B	A
1	1	1	1	1	1	1	1	1	1	1	1	1
0	1	1	1	1	1	1	1	1	1	1	1	0
x	0	1	1	1	1	1	1	1	1	1	0	1
x	x	0	1	1	1	1	1	1	1	1	0	0
x	x	x	0	1	1	1	1	1	1	0	1	1
x	x	x	x	0	1	1	1	1	1	0	1	0
x	x	x	x	x	0	1	1	1	1	0	0	1
x	x	x	x	x	x	0	1	1	1	0	0	0
x	x	x	x	x	x	x	0	1	0	1	1	1
x	x	x	x	x	x	x	x	0	0	1	1	0

iii) Write the difference between combinational and sequential logic circuit

Ans: (each correct point 1M)

	Combinational circuit	**Sequential circuit**
1	The output at any instant of time depends upon the input present at that instant of time.	The output at any instance of time depends upon the present input as well as past input and output.
2	No memory element required in the ckt	Memory element required to stored bit
3	Clock input not necessary	Clock input necessary
4	E.g. Adders, Subtractors ,Code converters , comparators etc.	E.g. Flip flop, Shift registers, counters etc,
5	Used to simplify Boolean expressions, k-map , Truth table	Used in counters & registers

2. Attempt any four of the following: **Marks 16**

a. Perform the following BCD operation

(i) $(37)_{10}+(65)_{10}$

(ii) $(46)_{10}-(73)_{10}$ use 10"s complement method.

Ans : (each correct answer 2M)

(i) $(37)_{10}+(65)_{10}$

```
    0011  0111
+   0110  0101
--------------
    1001  1100
```

Invalid BCD so correction of 6

```
    1001  1100
+   0000  0110
--------------
    1010  0010
```

Invalid BCD

So correction of 6

```
      1010  0010
+     0110  0000
----------------
   1  0000  0010
```

So Answer is $(102)_{10}$

ii)

(ii) Perform $(46)_{10} - (73)_{10}$ in BCD using 10's complement.

Step (i): Find 10's complement of $(73)_{10}$

9's complement of 73 → 99 − 73 = 26

Add 1 → + 1

27

Step (ii): Add $(46)_{10}$ to 10's complement of $(73)_{10}$ i.e. $(27)_{10}$.

Decimal		BCD	
$(46)_{10}$		0100	0110
$(27)_{10}$	+	0010	0111
		0110	1101

$\underbrace{1101}_{\text{Invalid}}$ Answer is negative and not in true form ∴ Take 10's complement

	+	0000	0110
Carry 0 → $\boxed{0}$		0111	0011

Taking 9's complement and adding

	1001	1001	
−	0111	0011	
	0010	0110	→ 9's complement
+		1	→ Adding 1
	$\underbrace{0010}_{2}$	$\underbrace{0111}_{7}$	

$\therefore (46)_{10} - (73)_{10} = (-27)_{10}$

b. Draw and explain the circuit diagram of 1:4 demultiplexer using logic gates.

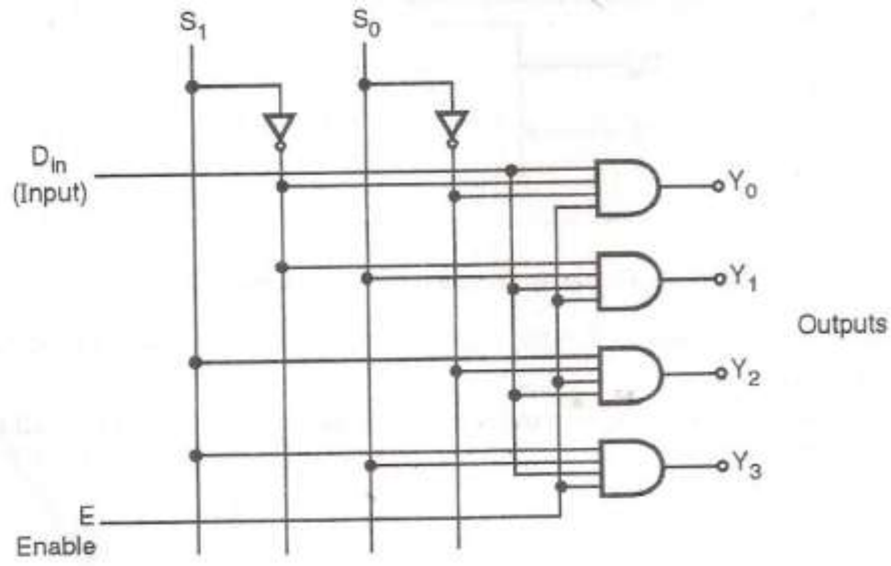
Ans: (circuit diagram 2M,truth table 1M,explanation 1M)

1:4 demultiplexer has only one data input D, two select inputs, one strobe E input and four outputsY0, Y1,Y2 and Y3.

The strobe input may be active low or active high and it is used for cascading.

The truth table is as shown below. From this table it is clear that D is connected to Y0 when S1S0=00, it is connected to Y1 when S1S0 = 01 and so on.

The other outputs will remain 0.Here the E input needs to be active high .If it is low all outputs will be 0 irrespective of any data input or select inputs



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TRUTH TABLE of 1:4 Demultiplexer

E	S0	S1	Y0	Y1	Y2	Y3
0	X	X	0	0	0	0
1	0	0	D_{in}	0	0	0
1	0	1	0	D_{in}	0	0
1	1	0	0	0	D_{in}	0
1	1	1	0	0	0	D_{in}

c. Why NOR gate is called as Universal gate? Implement basic gates using NOR gate.
Ans :(why NOR as universal gate 1M,implementation of gates 1M each)

With the help of NOR gate it is possible to implement all basic gates as well as exclusive gates hence it is called as Universal gate**.**

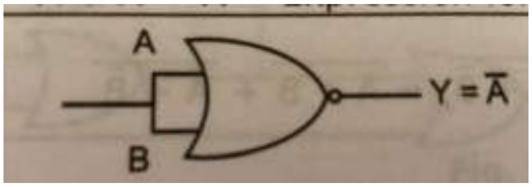


Fig: Implementation of NOT gate using NOR

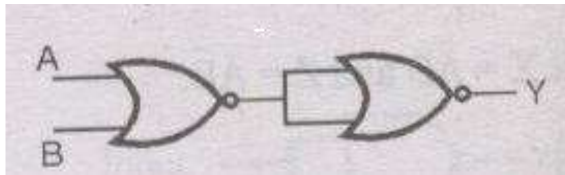


Fig: Implementation of OR gate using NOR

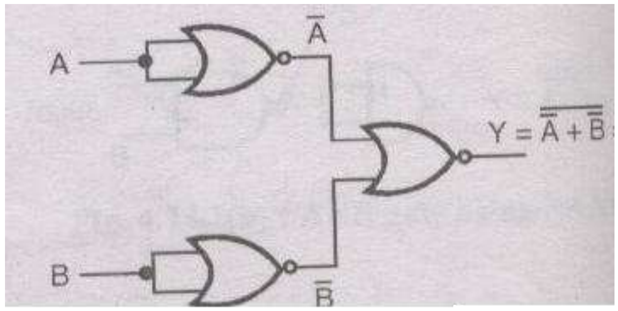
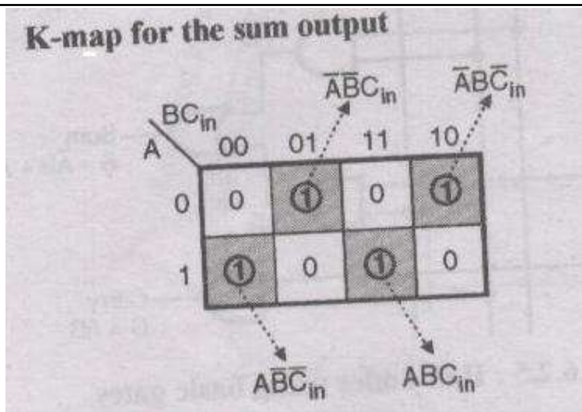


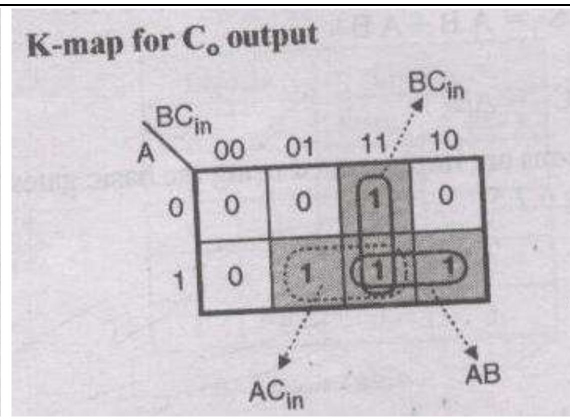
Fig: Implementation of AND gate using NOR

d. Explain full adder with is truth table, K-map specification and logic diagram.

Ans : (truth table 1M,Kmap specification 1M,equations 1M,logic diagram 1M)

Inputs			Outputs	
A	B	C_{in}	S	C_o
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1





$$S = \overline{A}\,\overline{B}C_{in} + \overline{A}B\overline{C}_{in} + ABC_{in} + A\overline{B}\,\overline{C}_{in}$$

$$S = C_{in}\underbrace{(\overline{A}\,\overline{B} + AB)}_{\text{EX-NOR}} + \overline{C}_{in}\underbrace{(\overline{A}B + A\overline{B})}_{\text{EX-OR}}$$

$$C_o = AB + AC_{in} + BC_{in}$$

$$\therefore S = C_{in}\,\overline{(\overline{A}B + A\overline{B})} + \overline{C}_{in}(\overline{A}B + A\overline{B})$$

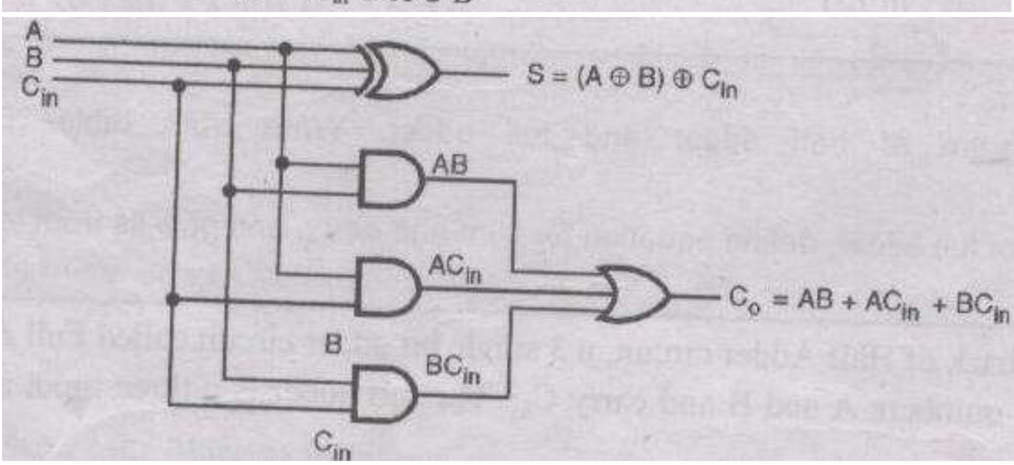
Let $X = \overline{A}B + A\overline{B}$

$$\therefore\ S = C_{in}\overline{X} + \overline{C}_{in}X = C_{in} \oplus X$$

$$\therefore\ S = C_{in} \oplus (\overline{A}B + A\overline{B})$$

But $\overline{A}B + A\overline{B} = A \oplus B$

$$\therefore\ S = C_{in} \oplus A \oplus B$$



e. Explain the working of 4 bit ring counter with a neat diagram.

Ans :(circuit diagram 2M,truth table 1M,explaination 1M)

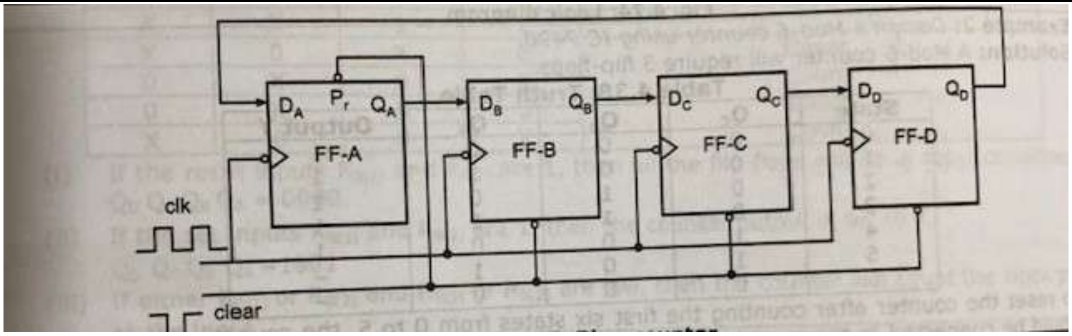
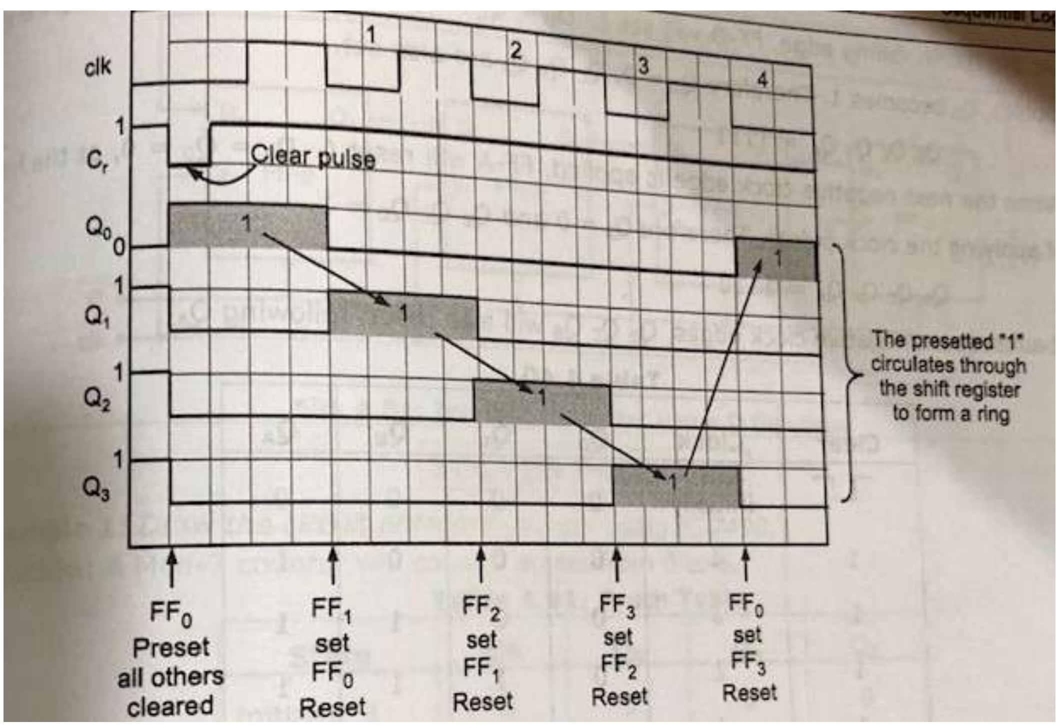


Table 4.39: Truth Table

clr	clk	Q_A	Q_B	Q_C	Q_D
⊔	X	1	0	0	0
1	↓	0	1	0	0
1	↓	0	0	1	0
1	↓	0	0	0	1
1	↓	1	0	0	0



Working:

A logic 0 to the clear terminal will reset the flip-flops B, C and D, whereas the Q_A output of FF-A will be set to logic 1 using the preset terminal.

$\therefore \quad Q_D\ Q_C\ Q_B\ Q_A = 0001$

The clear terminal is deactivated by applying a logic 1 signal to it. All the flip-flops are triggered simultaneously using the falling edge of the clock.

(i) When the first negative edge of the clock is applied, FF-B will set because $Q_A = D_B = 1$ and (at the instant of applying the clock Q_A was 1) FF-A will reset because $Q_D = D_A = 0$ (at the instant of applying the clock pulse Q_D was 0).

$\therefore \quad Q_D\ Q_C\ Q_B\ Q_A = 0010$

(ii) When the second negative edge of the clock is applied, only FF-C will set because $Q_B = D_C = 1$ and FF-B will reset because $Q_A = D_B = 0$.

$\therefore \quad Q_D\ Q_C\ Q_B\ Q_A = 0100$

(iii) When the third negative edge of the clock is applied, only FF-D will set because $Q_C = D_D = 1$ and FF-C will be reset, because $Q_B = D_C = 0$.

$\therefore \quad Q_D\ Q_C\ Q_B\ Q_A = 0001$

f.Compare between R-2R ladder DAC and weighted resistor DAC.(any four points)
Ans : (correct comparison 1M each)

Sr No.	R-2R ladder DAC	Weighted Resistor DAC
1	Slightly complicated in construction	Simple construction
2	It requires resistors of only two values	It requires more than two resistor values
3	Two resistors per bit	One resistor per bit
4	Easy to expand for more no. of bits	Not easy to expand for more no. of bits

Q. 3 Attempt any FOUR of the following: 16

a) Convert the following:

i. $(5C7)_{16} = (\ ?\ )_{10}$

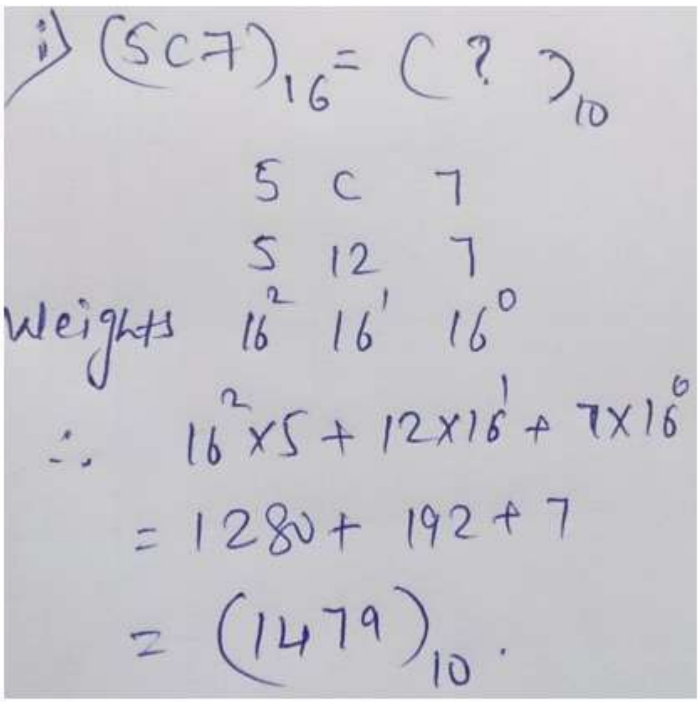
ii. $(1011.110)_2 = (\ ?\ )_{10}$

iii. $(43)_8 = (\ ?\ )_{10}$

iv. $(64C)_{16} + (\ ?\ )_2$

Ans :- Each proper answer 1mks

i. $(5C7)_{16} = (\ ?\ )_{10}$



i) $(5C7)_{16} = (\ ?\ )_{10}$

	5	C	7
	5	12	7
Weights	16^2	16^1	16^0

$\therefore\ 16^2 \times 5 + 12 \times 16^1 + 7 \times 16^0$

$= 1280 + 192 + 7$

$= (1479)_{10}$.

ii) $(1011.110)_2 = (\ ?\ )_{10}$

$$\begin{array}{cccccccc} 1 & 0 & 1 & 1 & \cdot & 1 & 1 & 0 \\ 2^3 & 2^2 & 2^1 & 2^0 & \cdot & 2^{-1} & 2^{-2} & 2^{-3} \end{array}$$

$$1\times2^3 + 0\times2^2 + 1\times2^1 + 1\times2^0 \cdot 1\times2^{-1} + 1\times2^{-2} + 0\times2^{-3}$$

$$8 + 0 + 2 + 1 \cdot \frac{1}{2} + \frac{1}{4} + 0$$

$$(11.75)_{10}$$

iii) $(43)_8 = (\ ?\ )_{10}$

$$\begin{array}{cc} 4 & 3 \\ 8^1 & 8^0 \end{array}$$

$$4\times8^1 + 3\times8^0 = (35)_{10}$$

iv) $(6AC)_{16} = (\ ?\ )_2$

$$\begin{array}{ccc} 6 & A & C \\ \downarrow & \downarrow & \downarrow \\ 6 & 10 & 12 \\ \downarrow & \downarrow & \downarrow \end{array}$$

$$(0110\ 1010\ 1100)_2$$

b) Simplify the following equations with Boolean Law.

(i) $y = A\overline{B} + \overline{A}B + AB + \overline{A}\,\overline{B}$

(ii) $y = A\overline{B}C + \overline{A}BC + ABC$

Ans:- Each simplification- 2 mks

i)

$$A\overline{B} + \overline{A}B + AB + \overline{A}\,\overline{B}$$

i) $A\overline{B} + \overline{A}B + AB + \overline{A}\,\overline{B}$

$= A\overline{B} + AB + \overline{A}B + \overline{A}\,\overline{B}$

$= A(\overline{B} + B) + \overline{A}(B + \overline{B})$ $\quad\because B + \overline{B} = 1$

$= A + \overline{A}$

$= 1$ $\quad\because A + \overline{A} = 1$

ii)

$$Y = A\bar{B}C + \bar{A}BC + ABC$$
$$= A\bar{B}C + BC(\bar{A} + A)$$
$$= A\bar{B}C + BC \qquad (\because \bar{A} + A = 1)$$
$$= C(B + A\bar{B})$$
$$= C(B + A)(B + \bar{B}) \quad \text{(distibutive law)}$$
$$= \underline{AC + BC}$$

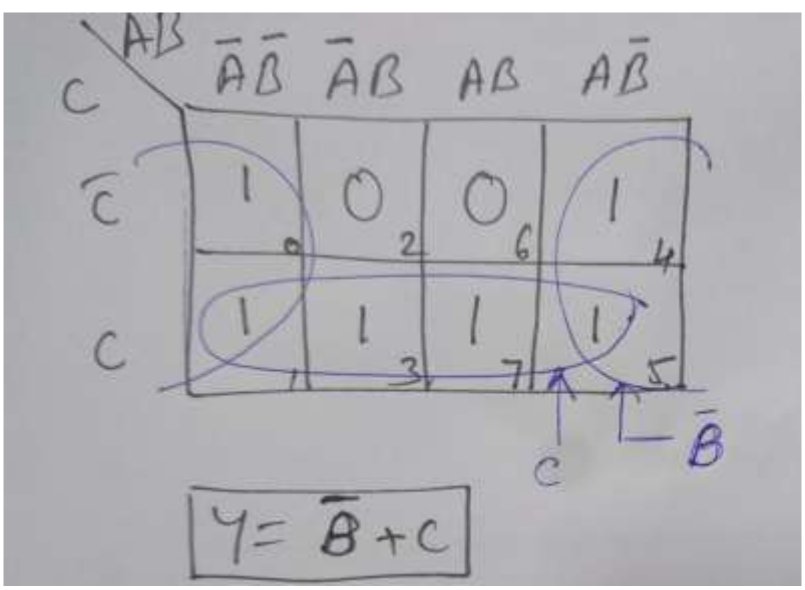
c) Minimize the following expression using K –map.

i. F(A, B, C) = Σm (0, 1. 3, 4. 5. 7)

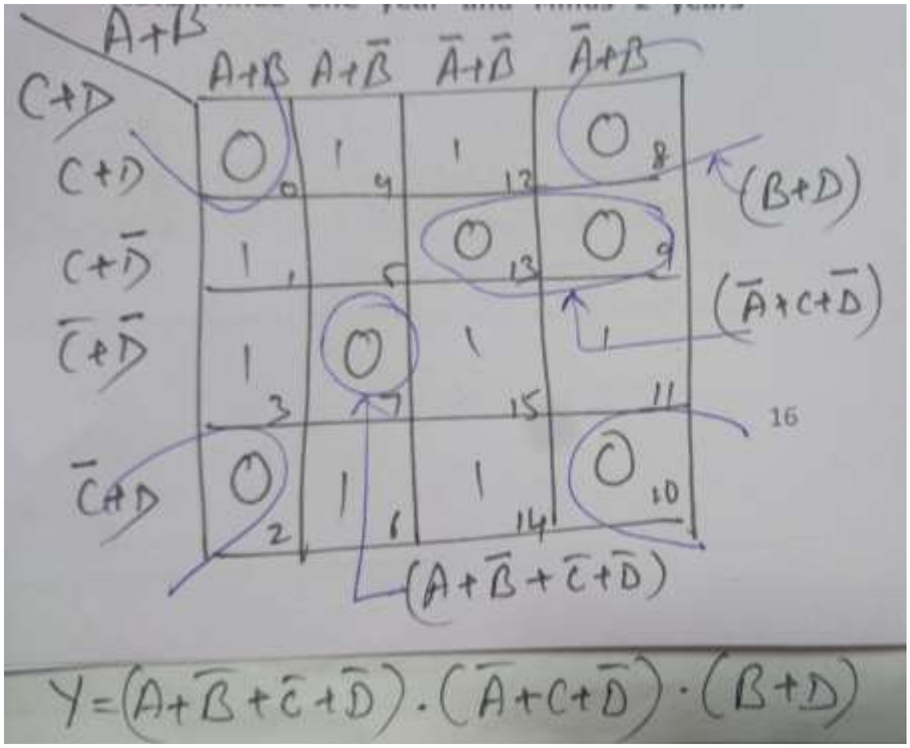
ii. F(A, B, C, D) = π M (0, 2, 7, 8, 9, 10, 13)

Ans:- Each minimization- 2 mks

i. F (A, B, C) = Σm (0, 1. 3, 4. 5. 7)



iii. F(A, B, C, D) = π M (0, 2, 7, 8, 9, 10, 13)



d) Identify the following circuit as combinational circuit OR sequential circuit.

i. 3 bit ring counter
ii. Dull Adder
iii. Clocked J-K FF
iv. 4:1 Mux

Ans : 1 mark each.

i) 3 – bit ring counter	=>	Sequential Circuit
ii) Full adder	=>	Combinational Circuit
iii) Clocked J-K F/F	=>	Sequential Circuit
iv) 4 : 1 MUX	=>	Combinational Circuit

e) Describe the working of single slop ADC with block diagram.

Ans:- Diagram- 2 mks, explanation- 2 mks

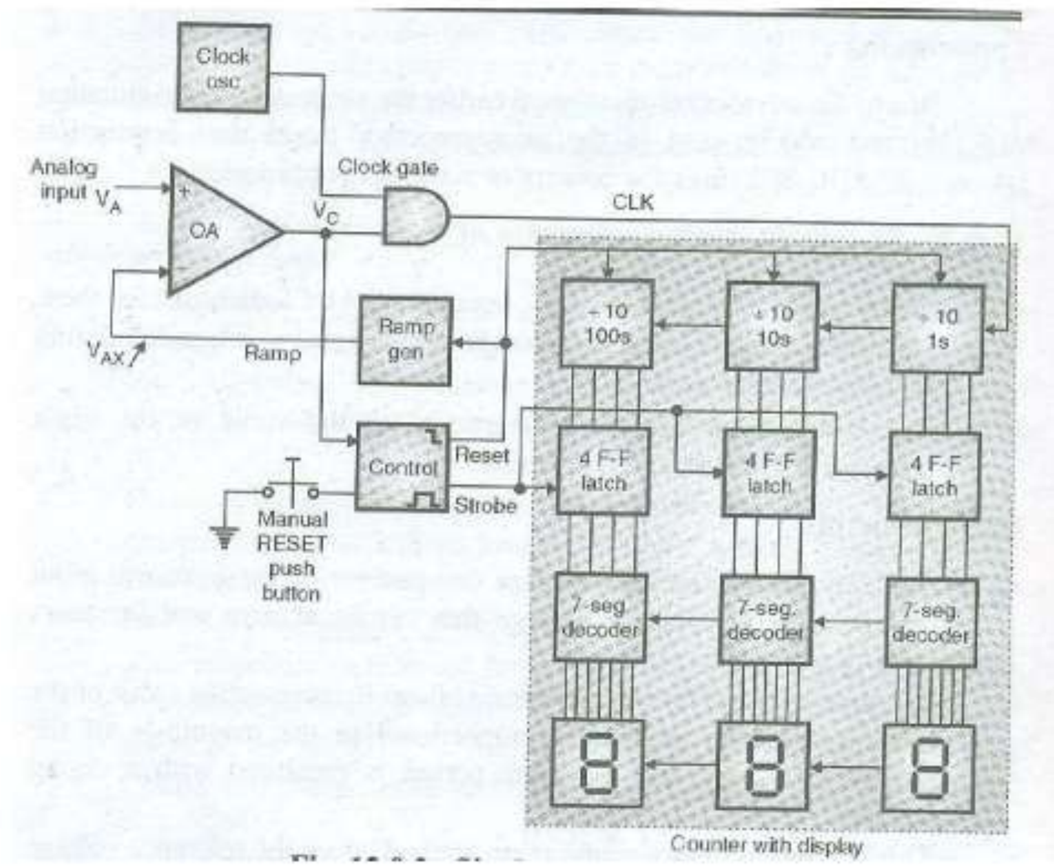
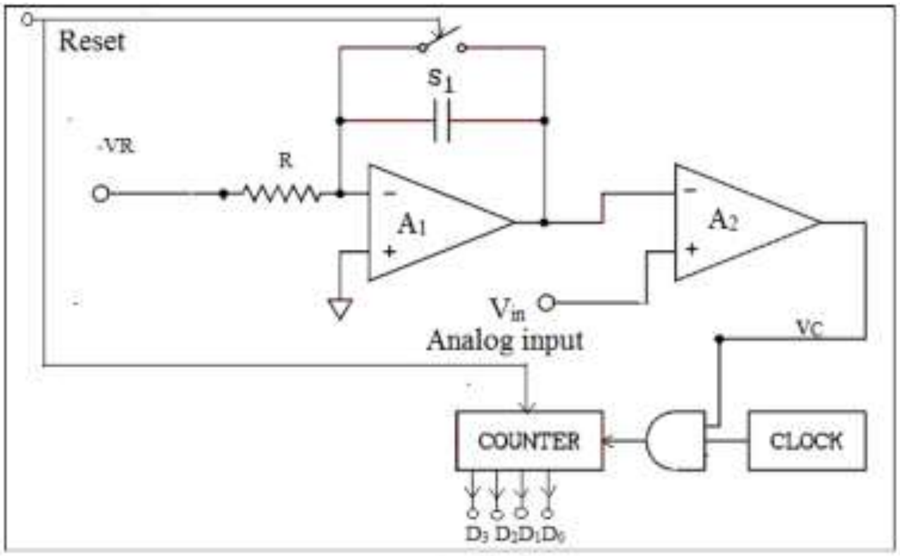


Fig: Single slope A/D converter

OR



Digital Output

Operation:

Manual RESET, will reset ramp generator as well as counter. V_A has to be positive. RAMP begins at 0V.

As $V_{AX} < V_A, V_C = 1$ (HIGH). This will enable CLOCK gate allowing the CLK input, to be applied to the counter.

The ramp generator may be of two types.

(a) Using DAC : This will resemble with counter-ramp ADC.

(b) Using a sample integrator : For integrator, if V_i is constant, the output voltage is given by equation $V_O = (V_i / RC)$. Since V_i, R and C are all constants, this is the equation of a straight line that has a slope (V_i / RC).

As counter receives clock pulses, it will count up; and the RAMP continues upward.

RAMP voltage rises till it reaches to V_A input voltage.

At this point, time t_1, output $V_O = 0$(LOW) and it will disable CLOCK gate and counter cease to advance.

The negative transition of V_O, simultaneously generates a strobe signal in the CONTROL box that shifts the contents of the three decade counters into the three 4 FF latch circuit,

Shortly after that, a reset pulse is generated (time t_2), by the CONTROL box that resets the RAMP and clears the decade counter to all 0's (ZEROS) and another conversion cycle begins.

In the meantime the contents of the previous conversion are contained in the latches and are displayed on the seven segment display.

f) State different types of ROM and explain any one in detail.

Ans:- Types-2 mks, explain any one -2 mks

There are five basic ROM types:

1. ROM - Read Only Memory.
2. PROM - Programmable Read Only Memory.
3. EPROM - Erasable Programmable Read Only Memory.
4. EEPROM - Electrically Erasable Programmable Read Only Memory.
5. Flash EEPROM memory.

Explanation :- (any one)

Flash Memory:-

1. Flash memory is non-volatile RAM memory that can be electrically erased and reprogrammed.
2. Flash memory can be written to in block size rather than bytes; it is easier to update it.
3. Due to this, the flash memories are faster than EEPROMS which erase and write new data of byte level.
4. This type of memory has been named as 'flash memory' because a large block of memory could be erased at one time, i.e. in a single action or 'flash'.
5. Important features are high speed, low operating voltage low power consumption.
6. Typically applications areas are digital camera`s embedded controllers, cellular phones etc.

OR

Programmable Read Only Memories (PROM):-

PROM is electrically programmable i.e. the data pattern is defined after final packaging rather than when the device is fabricated. The programming is done with an equipment referred to as PROM programmer. The PROM are one time programmable. Once programmed, the information stored is permanent.

OR

Erasable Programmable Read Only Memories (EPROM):-

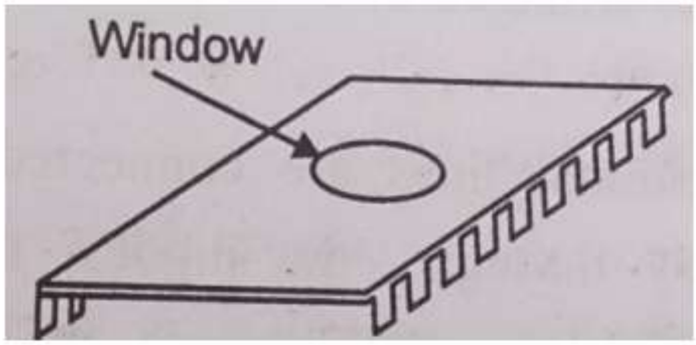
In these memories, data can be written in any number of times i.e. they are reprogrammable . Reprogrammable ROMs are possible only in MOS technology. For erasing the contents of the memory, one of the following two methods are employed:

a) Exposing the chip to ultraviolet radiation for about 30minutes (UVEPROM)
b) Erasing electrically by applying voltage of proper polarity & amplitude. Electricity erasable Prom is also referred to as E^2PROM or EEPROM or EAROM (Electrically alterable ROM)

In this data is stored in the form of charge.

OR

UV PROM- Ultra violet PROM-It can be erased by exposing the EPROM chip to ultraviolet sun rays. This EPROM has a quartz lid or window on the package as shown. we can erase the contents by exposing it to the ultraviolet rays for about 10-15 minutes, by which all the cells will be erased and all the locations will have the store as 1.



4. Attempt any FOUR of the following: 16

a) Convert the following numbers into binary and add them. $(173)_8$ + $(741)_8$

Ans. 4 Marks correct Answer

$(173)_8 = (011\ 111\ 011)_2$ $(741)_8 = (111\ 100\ 001)_2$

Add both the numbers

Carry	1	1	1	1				1	1	
+A		0	0	1	1	1	1	0	1	1
+B		1	1	1	1	0	0	0	0	1
	1	0	0	1	0	1	1	1	0	0

Writing in to octal form-

001 001 011 100 = $(1134)_8$

b) Compare Totem pole and Open Collector outputs. (any four points)

Ans:- Relevant 4 points- 4 mks

Parameter	Totem-Pole	Open Collector
1)Circuit components on the O/P side	Q3 (pull up transistor),D & Q4 (pull down transistors)are used.	Only the pull down transistor Q4 is used.
2)Wired ANDing	Cannot be done	Easily be done
3)External pull up resistor	Not required	Required to be connected
4)Speed	Operating speed is high	Operating speed is low
5)Power Dissipation	Low	High

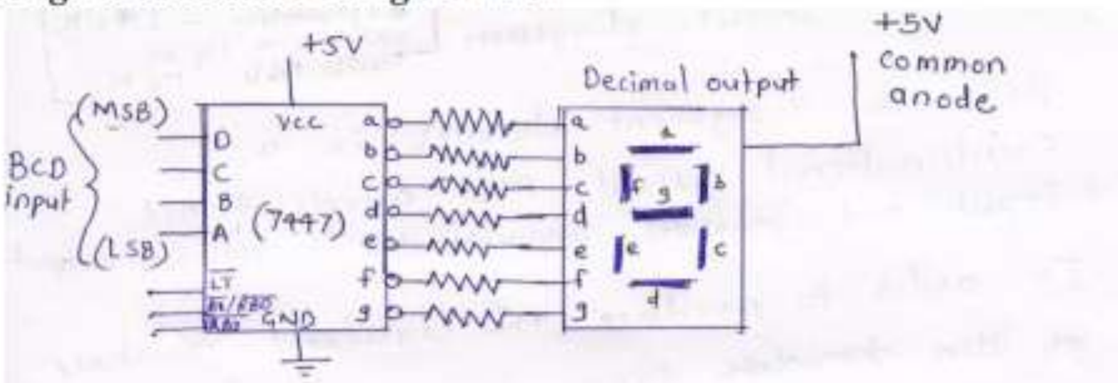
c) Describe the working of BCD to 7 segment decoder with truth table and circuit diagram.

Ans:- Diagram- 2 mks, explanation- 2 mks

- BCD to **7** segment decoder is a combinational circuit that accepts 4 bit BCD input and generates appropriate 7 segment output.
- In order to produce the required numbers from 0 to 9 on the display the correct combination of LED segments need to be illuminated.
- A standard 7 segment LED display generally has 8 input connections, one from each LED segment & one that acts as a common terminal or connection for all the internal segments
- Therefore there are 2 types of display
    1. Common Cathode Display
    2. Common Anode Display

Circuit diagram:-

BCD to 7 segment decoder Using IC 7447



For normal Functioning $\overline{LT}$, $\overline{BI}/\overline{RBO}$ & $\overline{RBI}$ Should be connected to logic 1

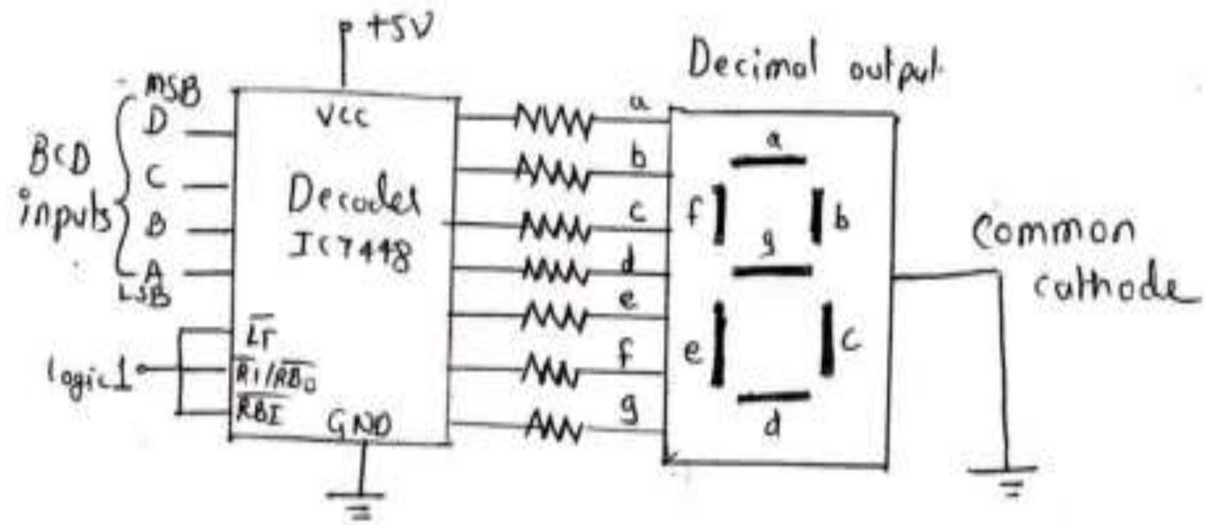
Observation Table

For seven segment decoder using common anode display

BCD Inputs				7 segment coded outputs							Display outputs
D	C	B	A	$\overline{a}$	$\overline{b}$	$\overline{c}$	$\overline{d}$	$\overline{e}$	$\overline{f}$	$\overline{g}$	
0	0	0	0	0	0	0	0	0	0	1	
0	0	0	1	1	0	0	1	1	1	1	
0	0	1	0	0	0	1	0	0	1	0	
0	0	1	1	0	0	0	0	1	1	0	
0	1	0	0	1	0	0	1	1	0	0	
0	1	0	1	0	1	0	0	1	0	0	
0	1	1	0	1	1	0	0	0	0	0	
0	1	1	1	0	0	0	1	1	1	1	
1	0	0	0	0	0	0	0	0	0	0	
1	0	0	1	0	0	0	1	1	0	0	

OR

BCD to 7 segment decoder Using IC 7448



BCD inputs				7 segment coded outputs							Display outputs
D	C	B	A	a	b	c	d	e	f	g	
0	0	0	0	1	1	1	1	1	1	0	0
0	0	0	1	0	1	1	0	0	0	0	1
0	0	1	0	1	1	0	1	1	0	1	2
0	0	1	1	1	1	1	1	0	0	1	3
0	1	0	0	0	1	1	0	0	1	1	4
0	1	0	1	1	0	1	1	0	1	1	5
0	1	1	0	0	0	1	1	1	1	1	6
0	1	1	1	1	1	1	0	0	0	0	7
1	0	0	0	1	1	1	1	1	1	1	8
1	0	0	1	1	1	1	0	0	1	1	9

d) Draw 3 bit asynchronous up counter with truth table and timing diagram.

Ans:- Diagram- 2 mks, truth table- 1 mks, waveforms- 1 mks

Ans c. [2 M for Diagram; 1M for truth table; 1 M for Timing Diagram]

Note: Weightage is to be given if diagram is drawn using T- flip flop in Toggle mode.

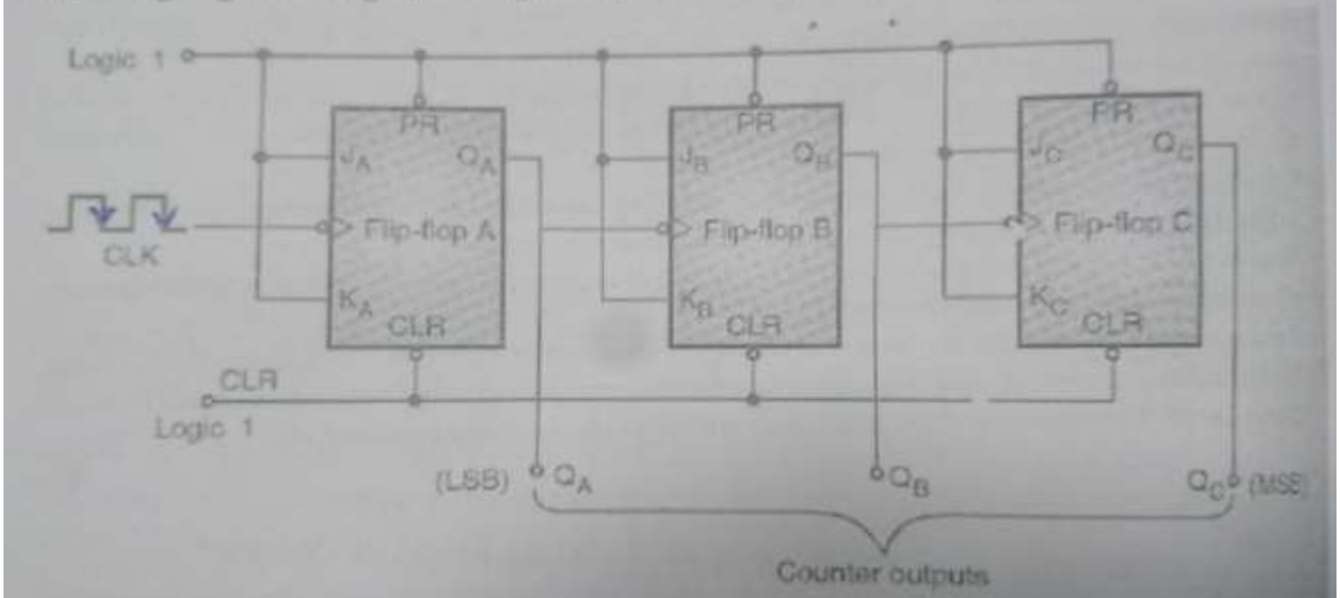


Fig: 3 bit asynchronous up counter

Clock	Flip-flop outputs			State	Decimal equivalent
	Q_C (MSB)	Q_B	Q_A (LSB)		
Initially	0	0	0	1	0
1^{st} (↓)	0	0	1	2	1
2^{nd} (↓)	0	1	0	3	2
3^{rd} (↓)	0	1	1	4	3
4^{th} (↓)	1	0	0	5	4
5^{th} (↓)	1	0	1	6	5
6^{th} (↓)	1	1	0	7	6
7^{th} (↓)	1	1	1	8	7
8^{th} (↓)	0	0	0	1	0

Fig: Truth Table.

Waveforms-

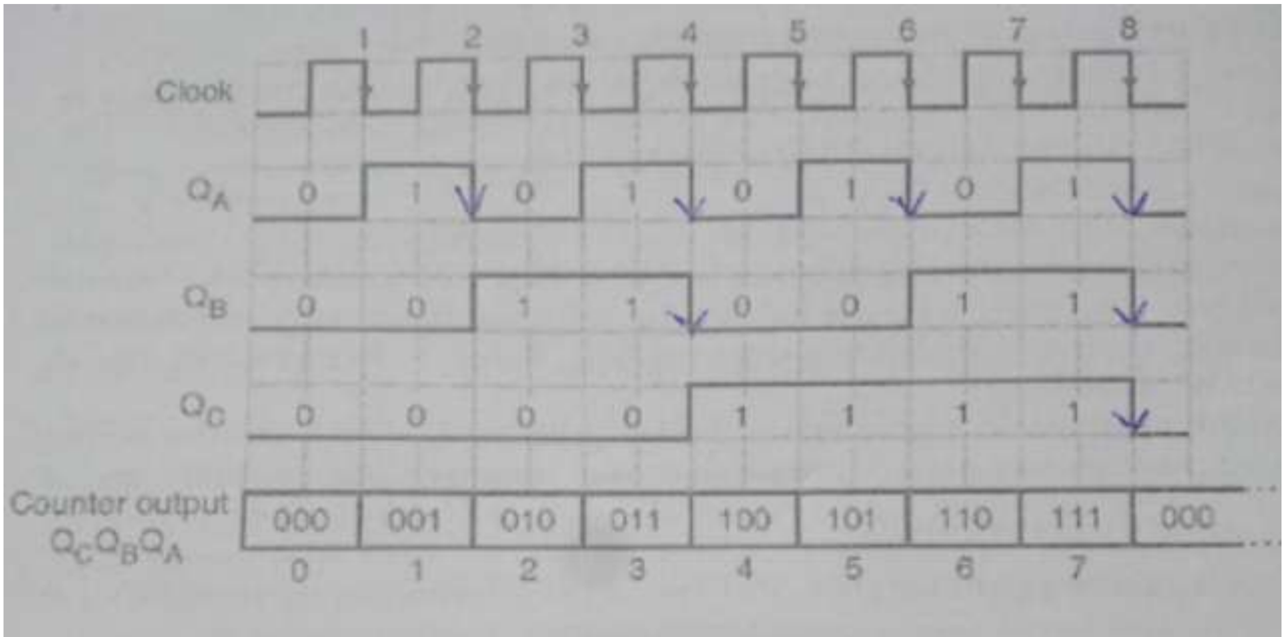
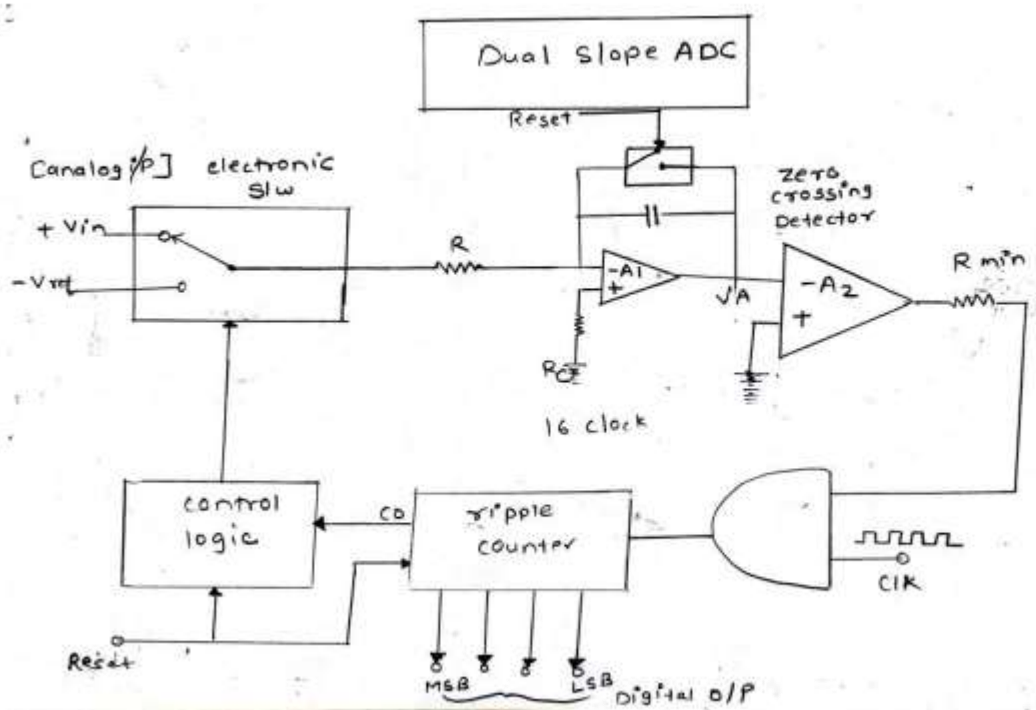


Fig: Timing diagram for a 3 bit asynchronous up counter

e) Describe the working of Dual Slop ADC.

Ans:- Diagram-2 mks, explanation- 2 mks

Diagram:-



Working:-

The DC voltage to be converted by the dual slope converted by the slope converter ,Vin is fed to an integrator, which produces a ramp waveform output. The ramp signal starts at zero & increases for a fixed time interval, T1 equal to maximum count of the counter by the clock frequency. An 8 bit counter operating at 1 MHZ would there by cause T1 to be 8μs.The slope of the ramp is proportional to the magnitude of V_{in}. At this end of the interval T_1. The carry-out (C_0) bit of the ripple counter causes the switches to move the $-V_{ref}$ position. In this position a constant current source ($-V_{ref}/R$) begins to discharge capacitor C. The ripple counter is reset to zero when there is Co. The count continues until the zero crossing detector switches state as a result of capacitor C being discharge. The counter is stopped by the zero crossing detector& the resultant count is proportional to the input voltage.

$$\boxed{V_{in} = V_{ref}\ (tr / T_1)}$$

f) Compare Volatile and Non-volatile Memory. (any four points)

Ans:- Relevant 4 points- 4 mks

Parameter	Volatile	Non-Volatile
1. **Definition**	Information stored is lost if power is turned off	Information stored is not lost even if power goes off
2. **Classification**	All RAM's	ROM's, EPROM's
3. **Effect of power**	Stored information is retained only as long as power is ON	No effect of power on stored information
4. **Application**	For temporary storage of data	For permanent storage of data
5. **Devices used**	Volatile memory devices are mainly solid state devices	Non-volatile memory can be solid state, magnetic or optical
6. **Speed**	Volatile memory is very fast in data processing	Non-volatile memory is slow in data processing as compared to volatile

5. Attempt any FOUR of the following: 16

a) State and prove first and second De-morgan's theorem.

Ans : 2 Marks each theorem

i) $\overline{AB} = \overline{A} + \overline{B}$

It states that compliment of product is equal to sum of their compliments.

1	2	3	4	5	6
A	B	$\overline{AB}$	$\overline{A}$	$\overline{B}$	$\overline{A}+\overline{B}$
0	0	1	1	1	1
0	1	1	1	0	1
1	0	1	0	1	1
1	1	0	0	0	0

Column 03 = column 06
i.e. $\overline{AB} = \overline{A}+\overline{B}$
Hence proved

ii) $\overline{A+B} = \overline{A} \cdot \overline{B}$

It states that complement of sum is equal to product of their complements.

1	2	3	4	5	6
A	B	$\overline{A+B}$	$\overline{A}$	$\overline{B}$	$\overline{A} \cdot \overline{B}$
0	0	1	1	1	1
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	0

Column 03 = column 06
$\therefore \overline{A+B} = \overline{A} \cdot \overline{B}$
Hence proved.

b) Compare TTL and CMOS logic families on the basis of size, power consumption, speed, and fan out.

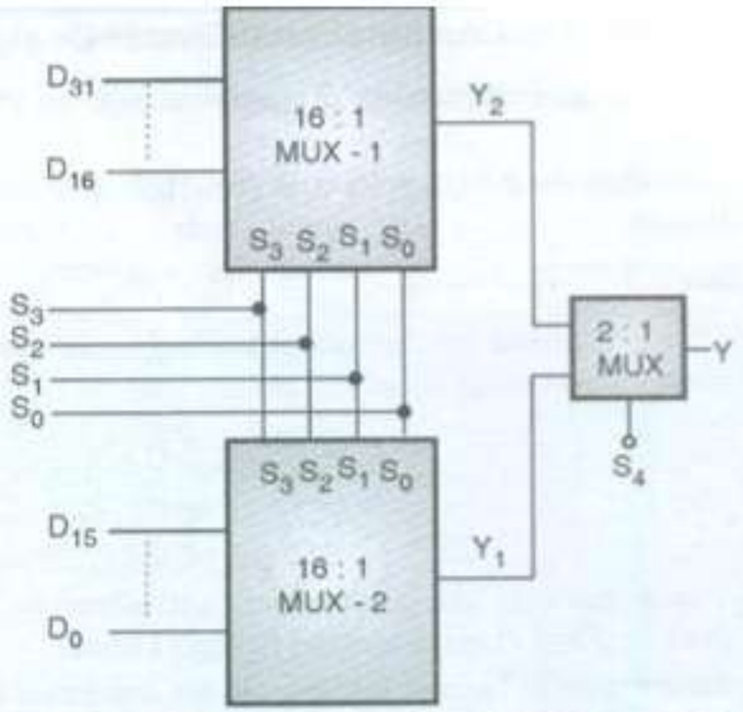
Ans:- Each comparison – 1 mks

Parameters	TTL	CMOS
Basis of size	Large	Small
Power consumption	10mW	10nW
Speed	Faster	Slower
Fan out	10	➢ 50

c) Design 32:1 multiplexer using 16:1 multiplexer and one 2:1 multiplexer.

Ans : Diagram : 4 marks.

Solution :



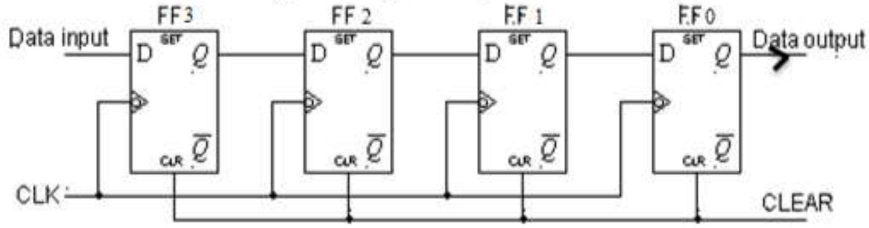
32:1 MUX using 16:1 MUX and 2:1 MUX

d) Draw logic diagram of 4 bit SISO shift register and its output waveform.

Ans:- Diagram- 2 mks, waveforms-2 mks

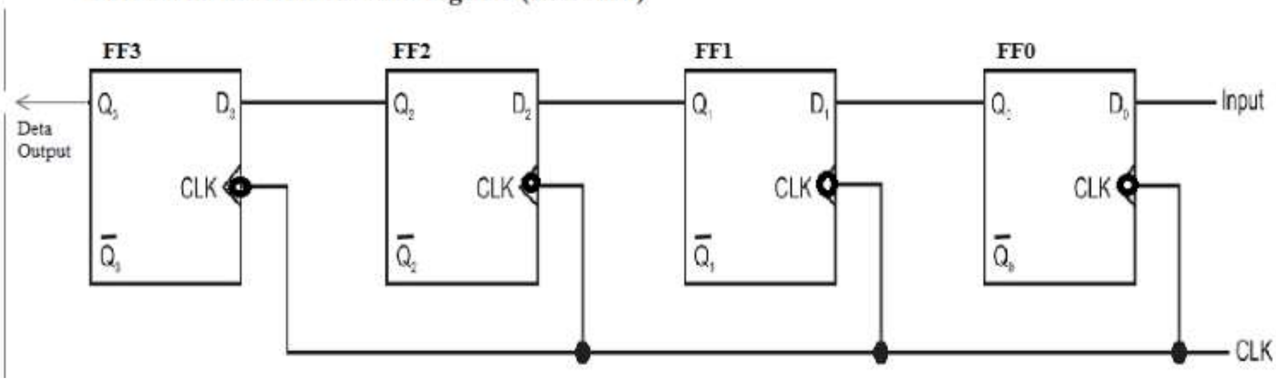
(SISO can be explained either for shift right or shift left)

Diagram:-4 bit Serial in serial out shift register (Right shift) **02M**

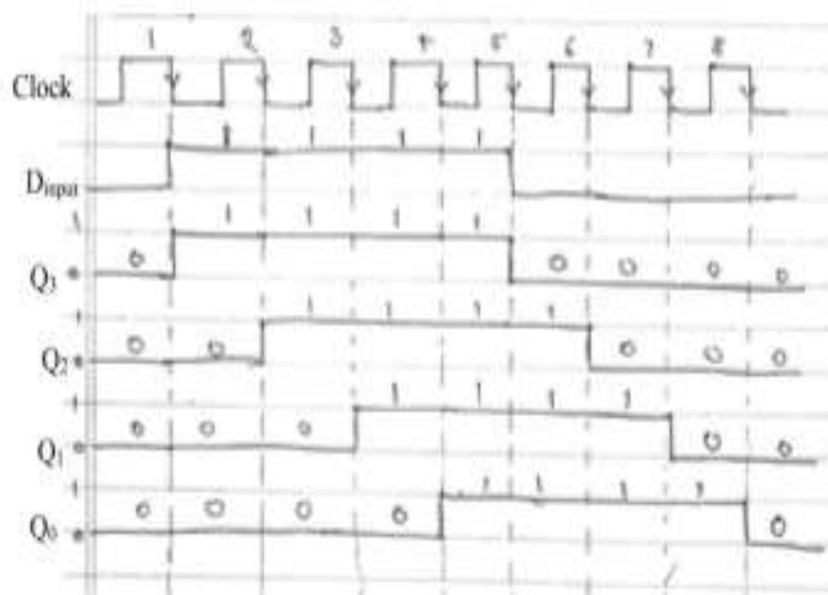


OR

4 bit Serial in serial out shift register (Left shift)



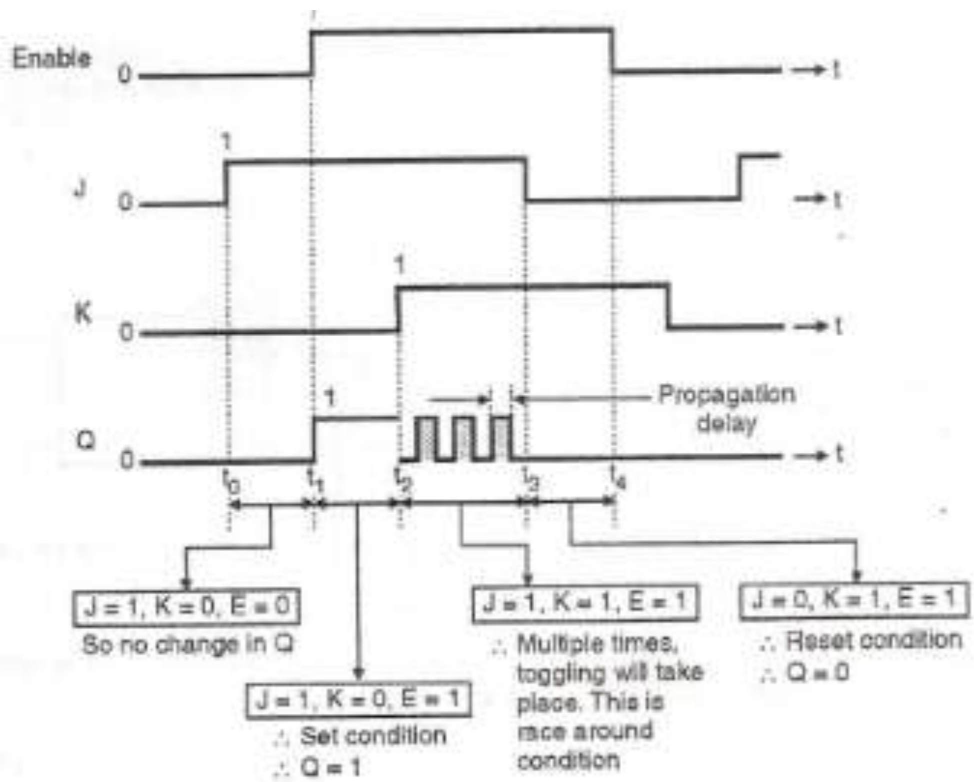
Waveform:- Right shift



e) What is race-around condition in J-K Flip Flop? How is it avoided using MS JK – Flip Flop?

Ans:- Race around condition- 2 mks, Avoided using master slave flipflop – 2 mks

Race around condition occurs in J K Flipflop only when J=K=1 and clock/enable is high (logic 1) as shown below-



Explanation:-In JK Flip-flop when J=K=1 and when clock goes high, output should toggle (change to opposite state) ,but due to multiple feedback output changes/toggles many times till the clock/enable is high. Thus toggling takes place more than once, called as racing or race around condition.

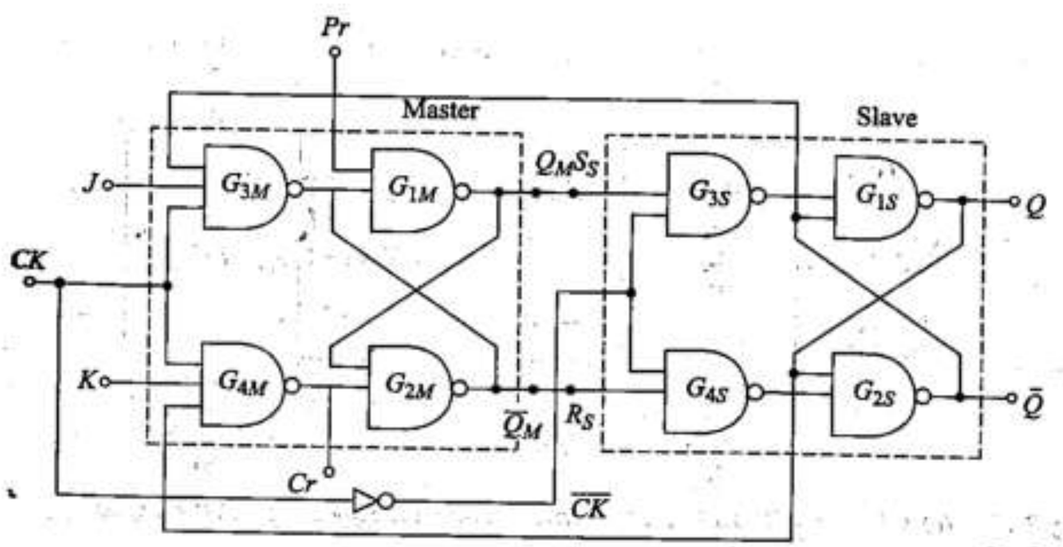
Master Slave JK Flip Flop **(2M)**

A master slave JK flip-flop is a cascade of two JK flip flops, with feedback from the output of the second to the inputs of the first. Positive clock pulses are applied to the first flip-flop and clock pulses are inverted before these are applied to the second flip-flop.

When clock = 1 the first flip flop is enabled and the outputs Q_m and $\overline{Q}_m$ respond to the inputs J and K.

At the same time, the second flip-flop is inhibited. When clk = 0, the second flip-flop is enabled and the first flip-flop is inhibited. Therefore the outputs Q and $\overline{Q}$ follow the output Q_m and $\overline{Q}_m$.

Since the second flip-flop simply follows the first one, it is referred to as the slave and the first one as the master. Hence the configuration is referred as master-slave (M-S) flip flop.



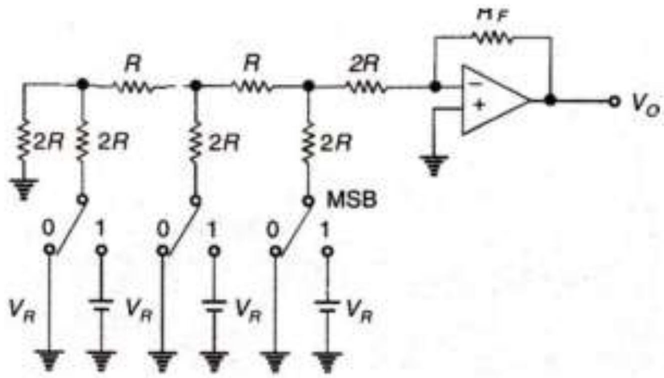
(Diagram can be exceptional)

f) Explain R -2R ladder network method of D\A conversion with neat circuit diagram.

Ans:- Diagram- 2 mks, explanation and derivation- 2 mks

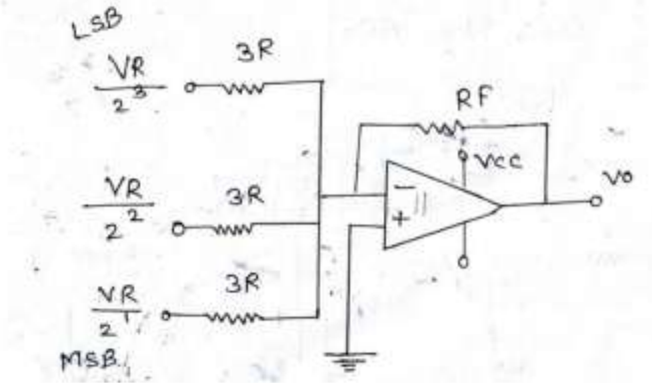
Consider a 3 bit (or n bit) DAC as shown-

Diagram:-



3 bit R-2R ladder network DAC

Mathematical derivation for Digital input 101:-



Equivalent 3 bit R-2R DAC

Where VR is the reference voltage

RF is the feedback resistor

3R is equivalent input resistance in each case

$$V_o = -\left(\frac{R_F}{3R}\frac{V_R}{2^3}b_0 + \frac{R_F}{3R}\frac{V_R}{2^2}b_1 + \frac{R_F}{3R}\frac{V_R}{2^1}b_2\right)$$

$$V_o = -\frac{R_F}{3R}\frac{V_R}{2^3}\left[b_0 + 2b_1 + 4b_2\right]$$

given i/p = 101 $\therefore \boxed{b_0 = 1, b_1 = 0, b_2 = 1}$

$$V_o = \frac{-R_F}{3R}\frac{V_R}{2^3}\left[1 + 0 + 4\right]$$

$$\boxed{V_o = 5\left[\frac{-R_F}{3R}\frac{V_R}{2^3}\right]}$$

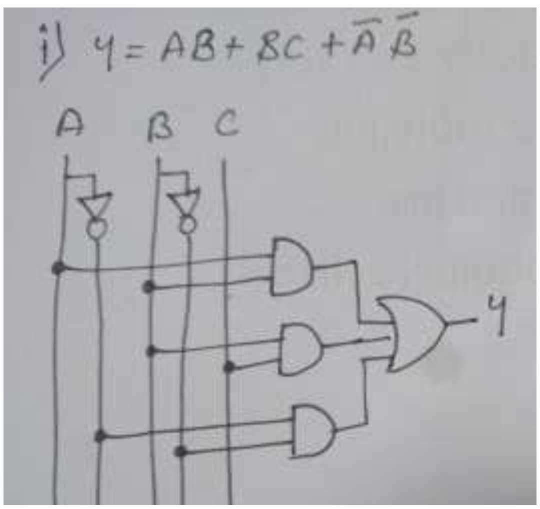
6. Attempt any FOUR of the following: 16

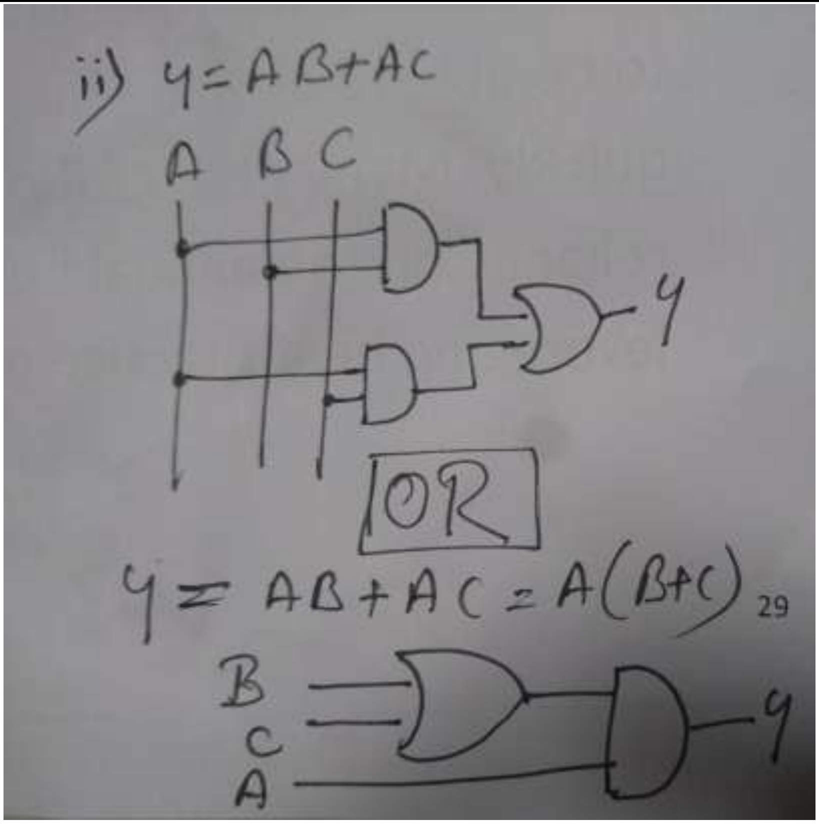
a) Realize the following Boolean expression using Basic gates.

(i) $y = AB + BC + \overline{A}\overline{B}$

(ii) $y = AB + AC$

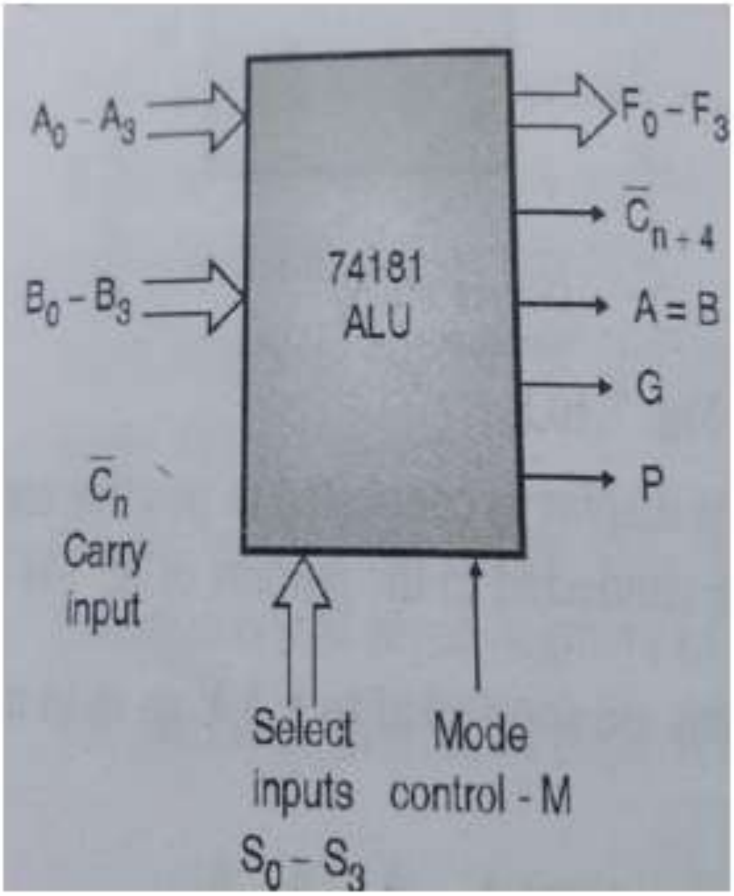
Ans:-Each realization- 2 mks





b) Draw the block diagram of ALU IC 74181 and also write its operation.

Ans- Diagram 2 mks, explanation 2 mks

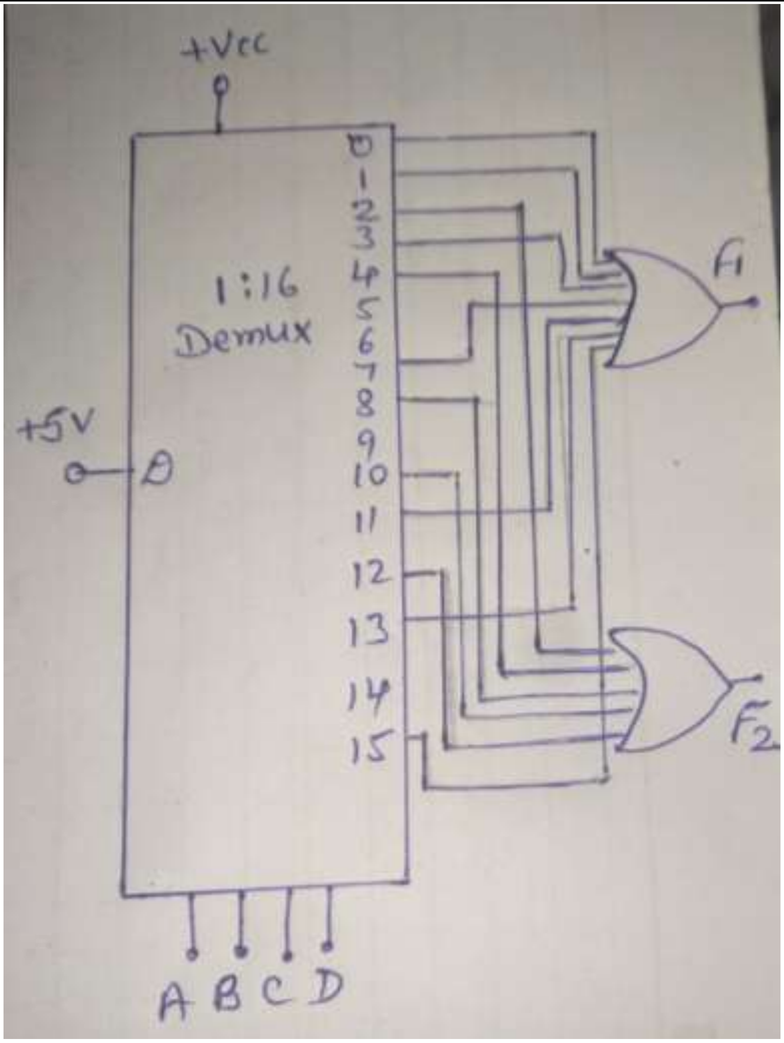


Explanation- IC 74181 is an high speed, 24 pin IC DIL package. widely used combinational logic, capable of performing the arithmetic as well as logical operations. It is the heart of microprocessor.
A and B are the two 4 bit input variables,
F is the 4 bit o/p variable, S are the 4 bit select lines that decides various (either arithematic as well as logical operations)
M= mode control that decides whether ALU will perform arithmetic or logical operations
If M= 1, Logical operations (16 AND,OR ,NOR etc operations ,depending upon the 4 bit combination of select lines)
If M=0, Arithmetic operations (16 addition, subtraction, division etc operations ,depending upon the 4 bit combination of select lines)
A=B ,Comparator equality o/p
G and P are the generate and carry propagate o/ps used for cascading of ALUs

c) Realize the following function using De-multiplexer.

i. $F_1 = \Sigma m\ (0, 1, 3, 7, 11, 13, 15)$
ii. $F_2 = \Sigma m\ (2, 4, 8, 10, 12)$

Ans:- Relevant and proper diagram- 4 mks



d) How IC 7490 can be used as a decade counter, explain with neat block diagram.

Ans:-(Explanation-1 mks , diagram -2 mks, truth table- 1mks)

Explanation- IC 7490-It consists of two counters namely MOD 2 and MOD 5. Thus IC 7490 can be used as MOD 2 or MOD 5 counter independently. Ehen this IC need to be used as MOD 10 ie decade counter, the o/p of MOD 2 counter ie QA need to be connected to the clock i/p of MOD 5 counter as shown below thus acting as a 4 bit MOD 10 counter.

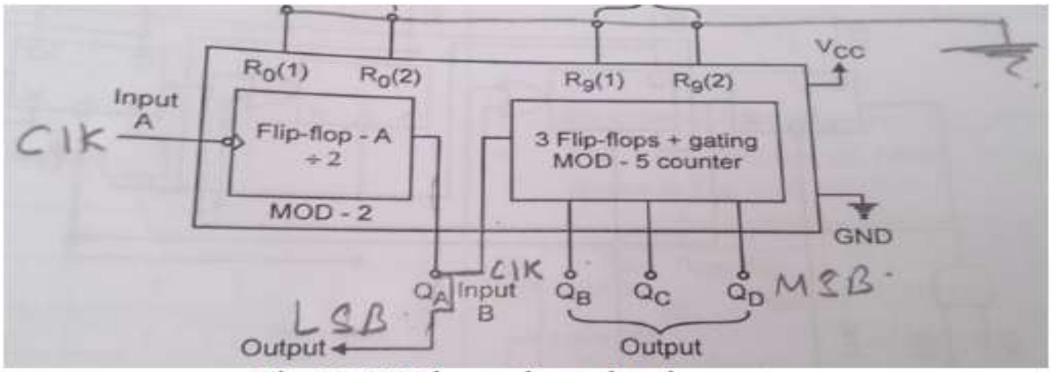


Fig: IC 7490 be used as a decade counter

Operation:-

Figure shows internal schematic of 7490 decade counter. It consist of four flip-flops internally connected to provide a mod-2 counter and a mod-5 counter . The mod-2 and mod-5 counters can be used independently or in combination. Flip flop FFA operates as mod-2 counter whereas the combination of flip-flop FFB, FFC and FFD form a mod-5 counter. There are two reset inputs R1 & R2 both of each are to be connected to logic 1 for clearing all the flip flops .the two set inputs s1 and s2 when connected to logic 1 are used for sitting the counter to 1001.

Truth	Table			
Decimal i/p	BCD/decimal o/p			
	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
0	0	0	0	0

e) Calculate the analog output of a 4 bit DAC if the digital input is 11101. Assume V_{FS} = 5V.

Ans:-Formula- 1 mks, proper solution 3 mks
Given:-The 4 bit digital word is
d1 d2 d3 d4 =1101 with V_{FS} = 5V ,to find V0-

$$V_o = V_{FS}\left[d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3} + d_4 2^{-4}\right]$$

$= 5(1*2^{-1} + 1*2^{-2} + 0*2^{-3} + 1*2^{-4})$

= 4.0625 Volts.

f) Compare static RAM and Dynamic RAM (any four points).

Ans:- Relevant comparison - 1 mks each

SR. NO.	PARAMETER	STATIC RAM	DYNAMIC RAM
1.	**Components**	Flip-flops, using bipolar or MOS transistors are used as basic memory cell.	Flip flops using MOS transistors& parasitic capacitance are used.
2.	**Refreshing**	Not required	Required as charge leaks
3.	**Speed**	Access time is less hence these are faster memories.	Access time is more hence these are slower memories.
4.	**Power Consumption**	More	Less
5.	**Space**	A Static RAM possesses more space in the chip than Dynamic RAM.	A Dynamic RAM possesses less space than a static RAM.
6.	**Cost**	More expensive	Less expensive.
7.	**Storage Capacity**	Less	High
8.	**No. of Components per cell**	More	Less
9.	**Bit Stored**	In the form of voltage.	In the form of charges.
10.	**Application**	Used in cars, household appliances, handheld electronic devices.	Used for computer memory.