WINTER– 18 EXAMINATION

Subject Name: Linear Integrated Circuits **Model Answer** Subject Code: 17445

Important Instructions to examiners:

1) The answers should be examined by key words and not as word-to-word as given in the model answer scheme.
2) The model answer and the answer written by candidate may vary but the examiner may try to assess the understanding level of the candidate.
3) The language errors such as grammatical, spelling errors should not be given more Importance (Not applicable for subject English and Communication Skills.
4) While assessing figures, examiner may give credit for principal components indicated in the figure. The figures drawn by candidate and model answer may vary. The examiner may give credit for any equivalent figure drawn.
5) Credits may be given step wise for numerical problems. In some cases, the assumed constant values may vary and there may be some difference in the candidate's answers and model answer.
6) In case of some questions credit may be given by judgement on part of examiner of relevant answer based on candidate's understanding.
7) For programming language papers, credit may be given to any other program based on equivalent concept.

1. a) Attempt any SIX of the following: 12

i) Define-
(1) CMRR
(2) Input Offset Voltage

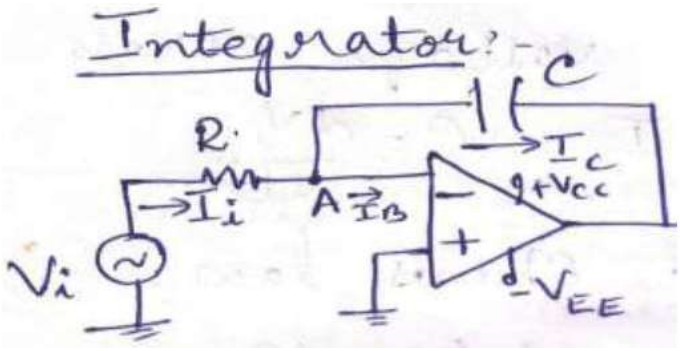
Ans: (1M for each definition.)

(1)CMRR: It defined as the ratio of differential gain to the common mode gain. It is the ability of an amplifier to reject the common mode signal.
Ideally CMRR= ∞.

(2)Input Offset Voltage: It is the input voltage that must be applied between both the input terminals of op- amp to make output offset voltage zero.
Ideally value of Input Offset Voltage is 0.

ii) Draw circuit diagram of basic integrator using op-amp.

Ans: (Correct diagram: 2M)



iii) State the need of signal conditioning.

Ans: (2M)

In an instrumentation system, a transducer is used for sensing various parameters. The output of transducer is an electrical signal proportional to the physical quantity sensed such as pressure, temperature etc.

However the transducer output cannot be used directly as an input to the rest of the instrumentation system.

In many applications, the signal needs to be conditioned and processed. The signal conditioning can be of different types such as rectification, clipping, clamping etc. Sometimes the input signal needs to undergo certain processing such as integration, differentiation, amplification etc.

iv) List any four specification of LM 324.

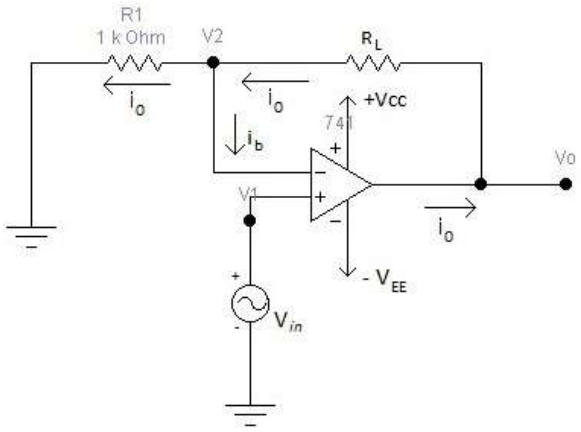
Ans: (2M for any 4 specifications)

1. Large DC voltage gain: 100dB

2. Wide bandwidth (unity gain): 1MHz (temperature-compensated)
3. Wide power supply range Single supply: 3VDC to 30VDC or dual supplies: ±1.5VDC to ±15VDC
4. Very low supply current drain: essentially independent of supply voltage (1mW/op amp at +5VDC)
5. Low input biasing current: 45nADC (temperature-compensated)
6. Low input offset voltage: 2mVDC and offset current: 5nADC
7. Differential input voltage range equal to the power supply voltage
8. Large output voltage: 0VDC to VCC-1.5VDC swing

v) Draw voltage to current converter with floating load.

Ans: (Correct diagram: 2M)



vi) Define-
(1) Q Factor of filter
(2) Roll of rate

Ans: (1M for each definition)

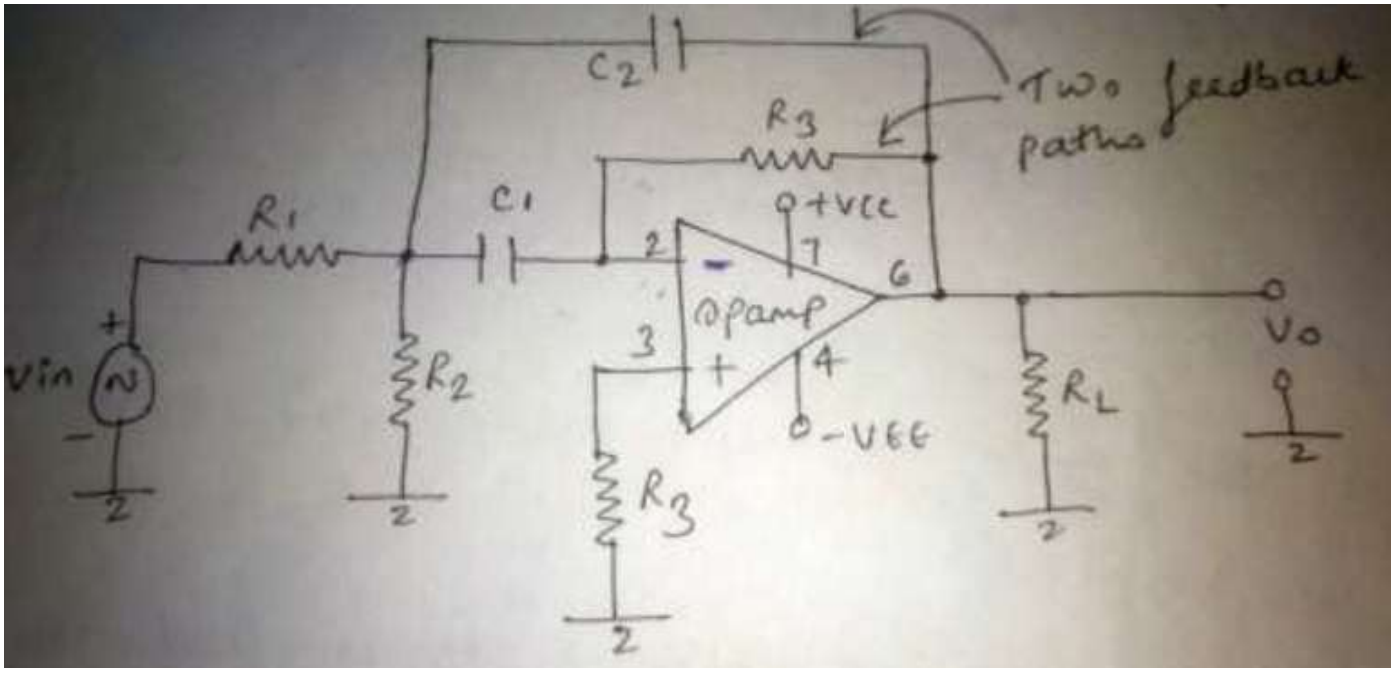
(1) Q Factor of filter: It is defined as the ratio of Centre frequency to the bandwidth

$Q=f_c/ BW$

(2)Roll of rate: The rate at which gain falls off rapidly in the stop band is called as Roll of rate

vii) Draw circuit diagram of narrow band pass filter using op-amp.

Ans: (Correct diagram: 2M)



viii) Draw pin diagram of IC 555.

Ans:- (IC pin diagram- 2 mks)

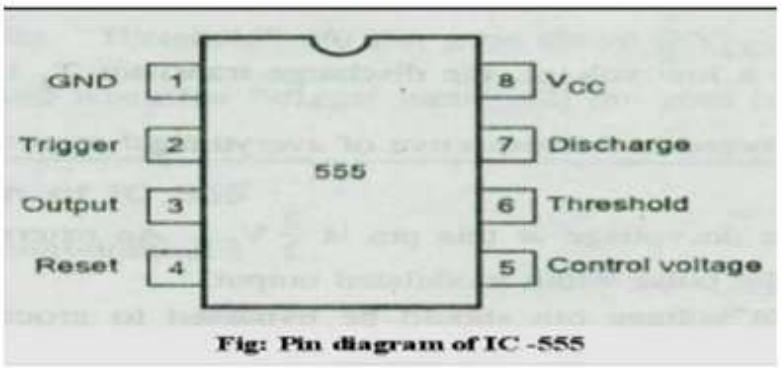


Fig: Pin diagram of IC -555

b) Attempt any TWO of the following: 8

i) Draw block diagram of op-amp. Describe the function of input stage and level shifting stage.

Ans: (correct diagram: 2M ; Function of each stage: 2M)

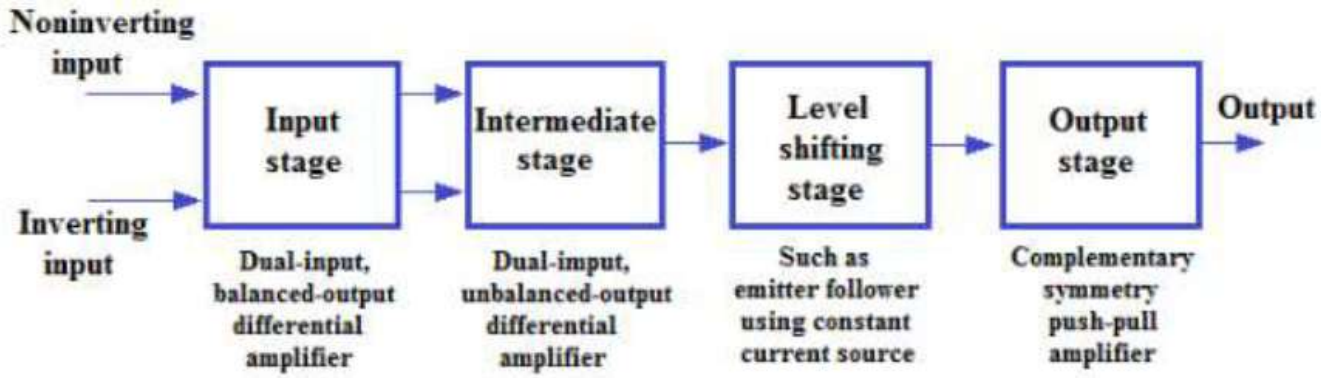


Fig: Block diagram of OP- AMP

Input Stage – The input stage is a dual input, balanced output differential. This stage provides most of the voltage gain of the OP-AMP and decides the input resistance value Ri.

Level shifting stage – Level shifting stage is used to bring dc level to zero volts with respect to ground.

ii) Compare ideal and practical op-amp values w.r.t.

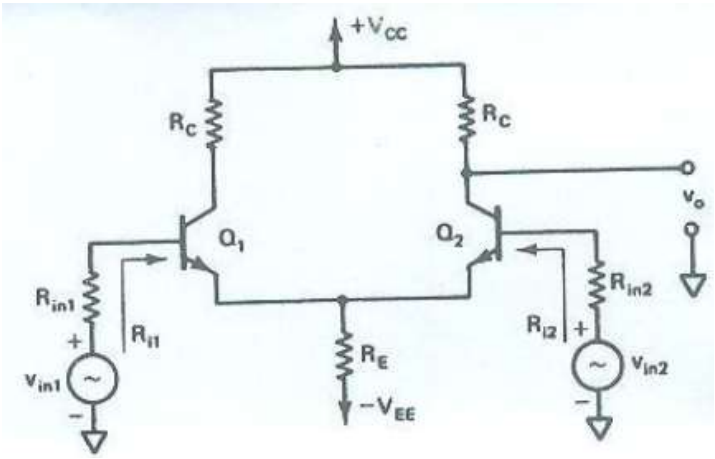
(1) SVRR
(2) Input offset voltage
(3) Input offset current
(4) Slew rate

Ans: (1M for each)

Sr. No.	Parameter	Ideal op-amp	Practical op-amp
1	SVRR	0	150V/µV
2	Input offset voltage	0	6mV
3	Input offset current	0	6nA
4	Slew rate	∞	0.5V/µs

iii) Draw dual input unbalanced output differential amplifier. State use of this stage.

Ans:(correct diagram:3M; Use: 1M)



Use of dual input unbalanced output differential amplifier: This stage provides additional gain, CMRR and isolation.

2. Attempt any FOUR of the following: **16**

a) Derive the equation of virtual ground concept in op-amp.

Ans: (Diagram:2M; Derivation: 2M)

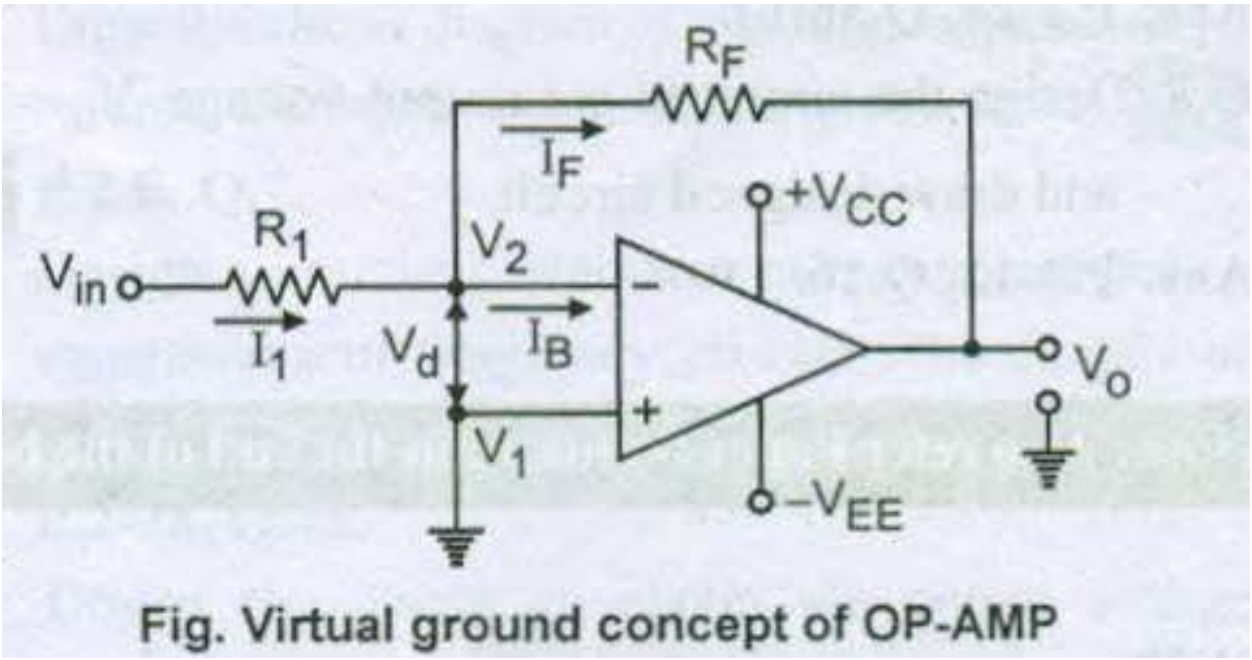


Fig. Virtual ground concept of OP-AMP

For op-amp,

$$V_d = V_1 - V_2$$

But, $A_V = \frac{V_0}{V_d}$

Ideally, $A_V = \infty$

$\therefore \quad V_d = 0$

$\therefore \quad V_1 - V_2 = 0$

$\therefore \quad \boxed{V_1 = V_2}$

b) Derive closed loop Inverting amplifier using op-amp and derive expression for its gain.

Ans:- (Diagram- 2 mks, derivation- 2 mks)

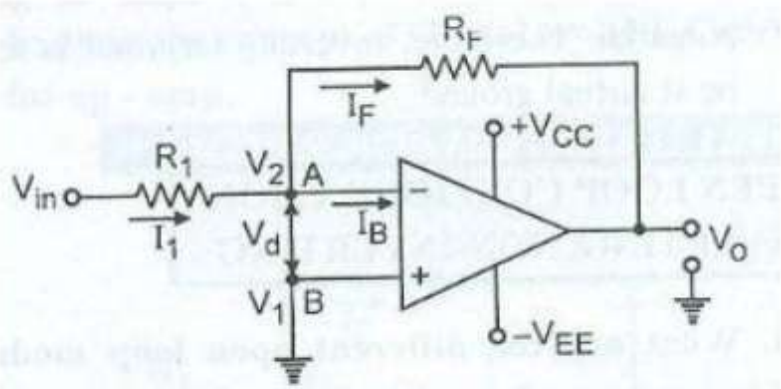


Fig. OP-Amp as an inverting amplifier

V_o= output voltage, V_{in}= input voltage, R_F= Feedback resistor, R_1= Input resistor

1. As input signal V_{in} is applied to inverting input, hence it is called as inverting amplifier and non inverting terminal is grounded.
2. The phase difference between input and output is 180^0
3. A negative feedback is provided from output to inverting terminal through R_F (Feedback resistor)

Derivation:

Apply KCL at node 'A', we get,

$$I_1 = I_B + I_f \quad \text{---- (1)}$$

But, $R_{in} = \infty$

$\therefore I_B = 0$

$\therefore I_1 = I_F$

$$\therefore \frac{V_{in} - V_2}{R_1} = \frac{V_2 - V_o}{R_F}$$

According to virtual ground condition,

$V_1 = V_2 = 0$

$$\therefore \frac{V_{in}}{R_1} = \frac{-V_o}{R_F}$$

$$\therefore \boxed{V_o = -\left(\frac{R_F}{R_1}\right) V_{in}} \quad \text{---- (2)}$$

$$\therefore \boxed{A_V = \frac{V_o}{V_{in}} = -\frac{R_F}{R_1}} \quad \text{---- (3)}$$

where, A_V = closed loop voltage gain

c) Design a circuit that convert square wave to triangular wave. Draw input –output waveforms.

Ans: (Design: 2M; Waveform: 2M)

The square wave input is mathematically represented as follows :

$$V_{in} = A \quad \text{... for } 0 \le t \le T/2$$

$$\text{and} \quad = -A \quad \text{... for } T/2 < t \le T$$

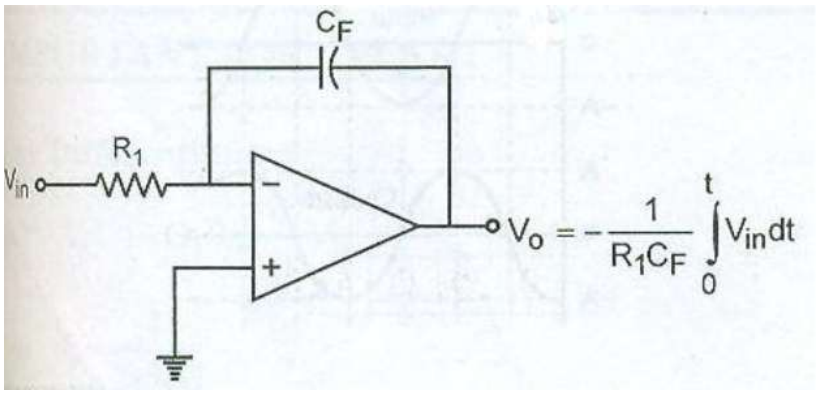
This expression is valid only for the first cycle.

This expression shows that the square wave is made of many step signals shifted in time. Hence for $V_{in} = A$ for $0 \leq t \leq T/2$ the output voltage will be a straight line with a slope – A

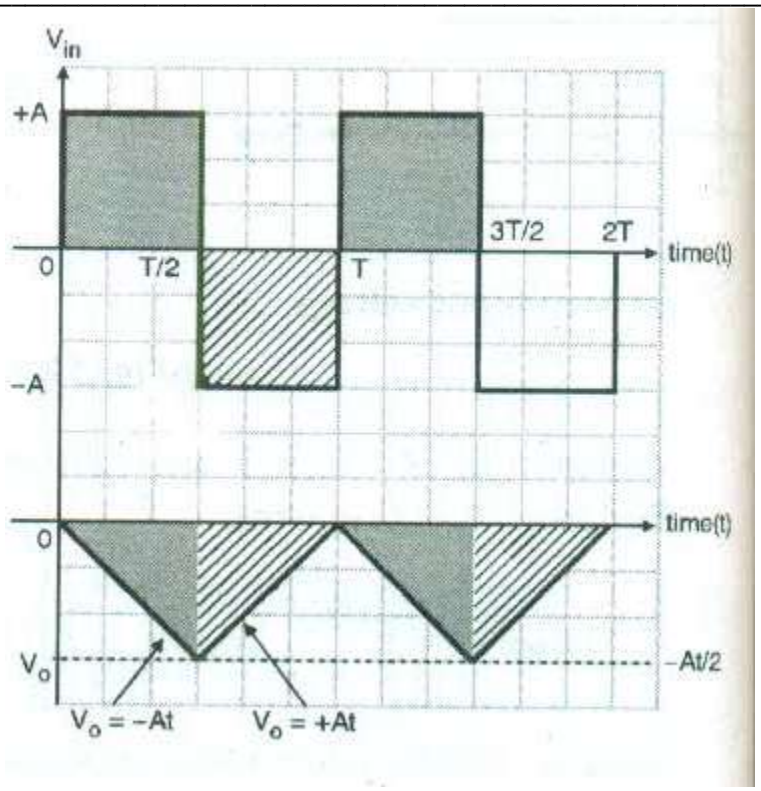
For $V_{in} = -A$ for $T/2 < t \leq T$, the output will be again a straight line with a slope of + A Thus for one cycle, the output voltage can be mathematically expressed as :

$$V_o = -At \quad \ldots 0 \leq t \leq T/2$$
$$\text{and} \quad = At \quad \ldots T/2 < t \leq T$$

with $R_1 C_F = 1$.



Waveform:



d) For unity gain amplifier if V_{in}=+5V. What will be the output voltage? Draw the circuit diagram of unity gain amplifier.

Ans: (correct ans: 2M; Diagram: 2M)

For unity gain amplifier, the input signal is applied at the non-inverting input of op-amp.

The gain of the unity gain amplifier is 1 i.e. unity.

Av= V_0/V_{in}

$V_0=V_{in}$

i.e. output voltage= input voltage

given V_{in}=+5V

then V_0= +5V.

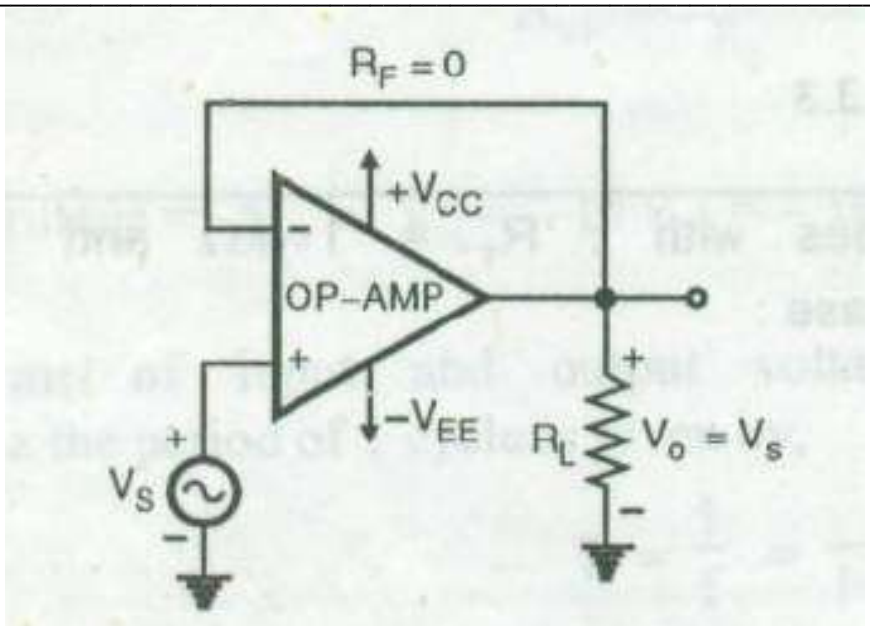


Fig: unity gain amplifier.

e) Draw basic differentiator. Derive the expression for relation between its input and output.

Ans: (Correct diagram: 2M; Expression: 2M)

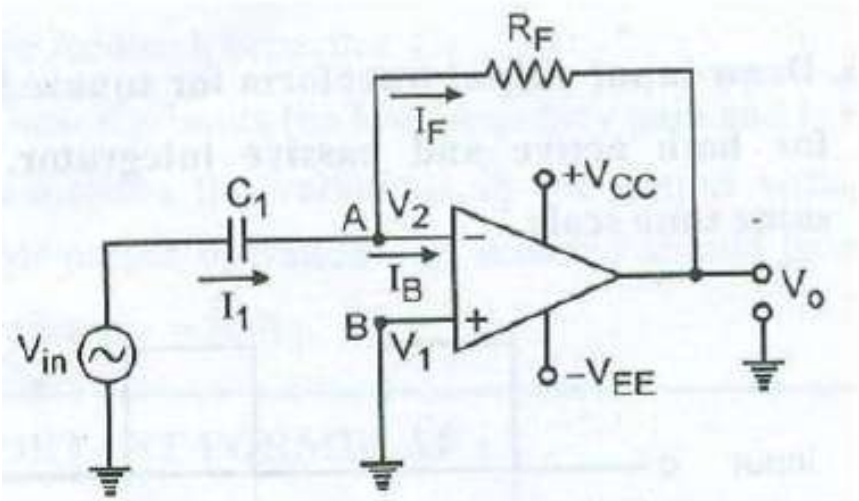


Fig. Circuit diagram of differentiator

Expression for relation between its input and output:

Applying KCL at node 'A'

$I_1 = I_B + I_f$

$\therefore R_{in} = \infty, I_B = 0$

$\therefore I_1 = I_f$

$$C_1 \frac{d}{dt}(V_{in} - V_2) = \frac{V_2 - V_o}{R_F}$$

Due to virtual ground condition

$V_1 = V_2 = 0$

$$\therefore C_1 \frac{d}{dt} V_{in} = -\frac{V_o}{R_F}$$

$$\therefore V_o = -R_F C_1 \frac{d}{dt} V_{in}$$

Negative sign indicates that it is an inverting amplifier and $V_o \propto \frac{d}{dt} V_{in}$.

f) Why offset nulling is required? Explain with circuit diagram.

Ans Need: 1M; Correct diagram: 2M; Explanation:1M)

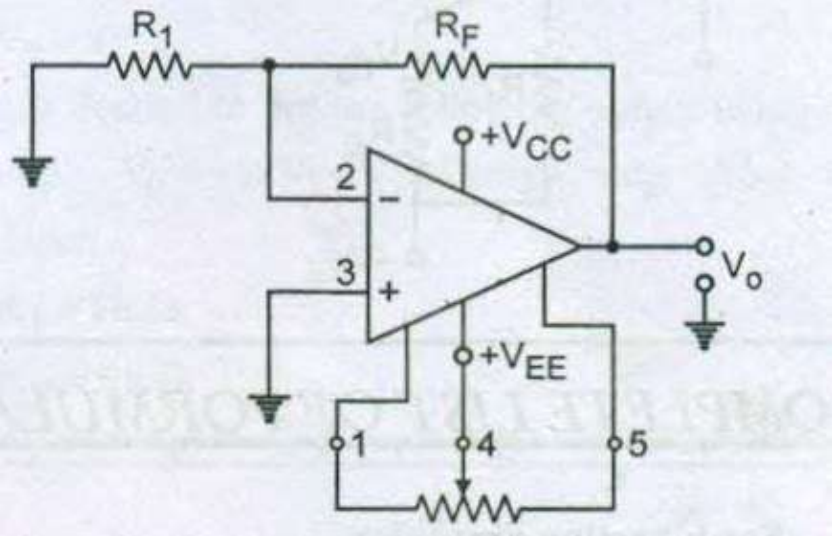
Need of offset nulling:

(1) To make output voltage zero, input voltage should be zero, but we get minimum (less) output voltage called as output offset voltage due to the presence of input offsest voltage at the input side.

(2) This input offset voltage is present even, when, both the input terminals are grounded.

(3) Hence, a technique is used to make output offset voltage zero. This technique is called as offset nulling technique.

Explanation:



In, this technique, a 10 kΩ potentiometer is connected between the offset null pins of IC741 i.e. pin no 1 and pin no. 5 and the wiper of potentiometer is connected to pin no.4 (i.e. $-V_{EE}$).
The wiper of potentiometer is varied in such a way that input offset voltage becomes zero.
Once input becomes zero, then output offset voltage also becomes zero.
Thus, the op-amp is said to the nulled or balanced.

3. Attempt any FOUR of the following: 16

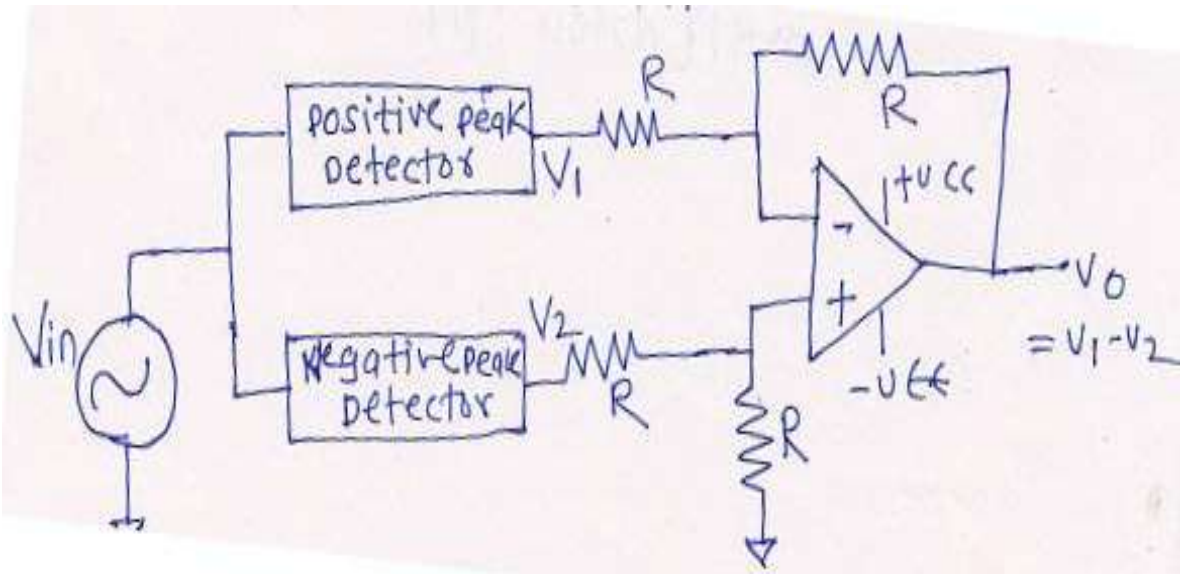
a) State the need of peak to peak detector and draw its circuit diagram.

Ans : (Needs-1 M, diagram-3M)

It is used to determine or detect the highest or maximum peak value of the input signal applied.

OR

It is used to determine the positive or negative peak **or** difference between the two peaks
Of the input signal.



b) Draw and explain circuit diagram of antilog amplifier.

Ans:- (Diagram- 2 mks, explanation/derivation 2 marks

$$I_f = I_o e^{V_{in}/\eta V_T}$$

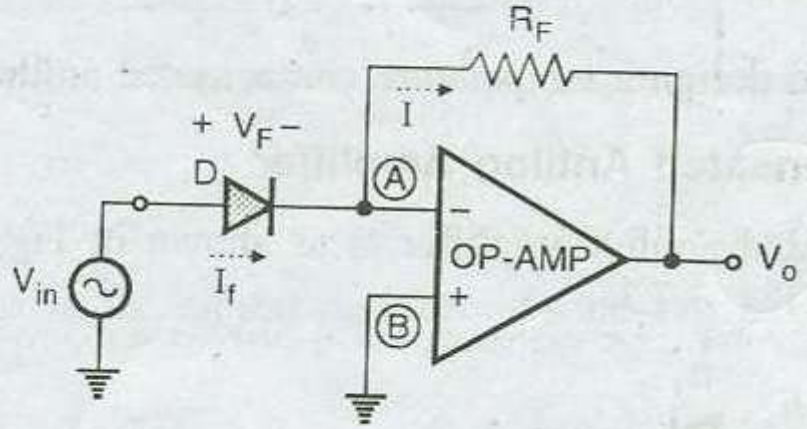


Fig. : Basic antilog amplifier using a diode

Operation: (2M)

Note that the diode and resistor in the log amplifier have interchanged their places.

As the non-inverting terminal B has been connected to ground, The inverting terminal A is also connected to the ground potential.

As point A is a virtual ground $V_{in} = V_F$. Therefore the expression for the forward current I_F through the diode is given by

- Assuming the input current of the OP-AMP to be zero, the current I flowing through the feedback resistor R_F is given by:

$$I = I_f = -\frac{V_o}{R_F}$$

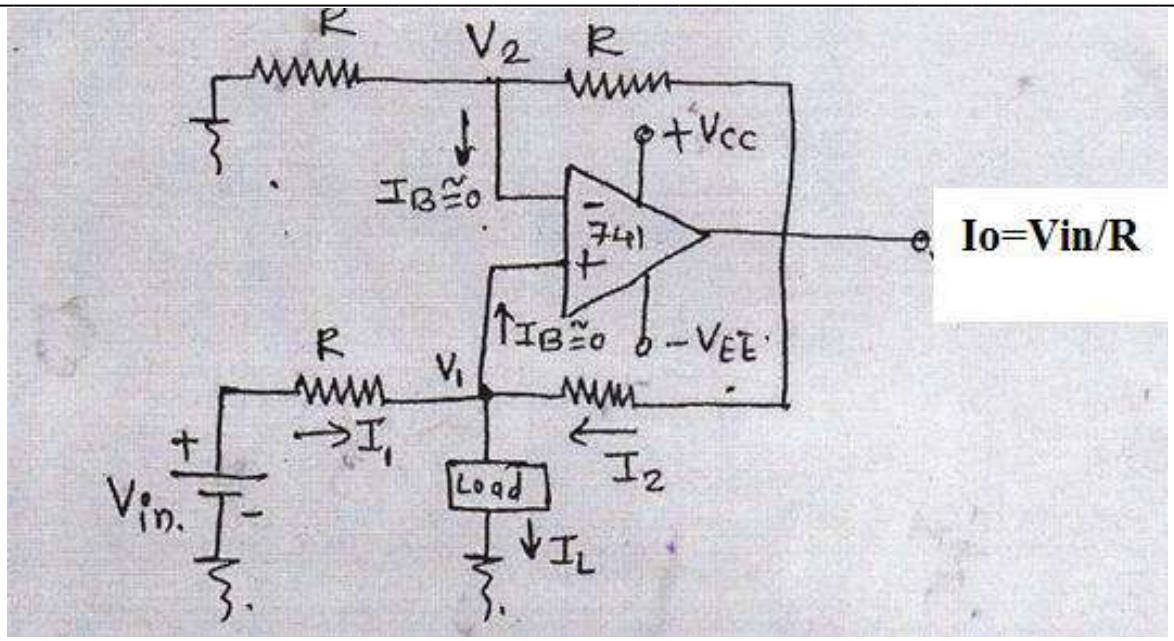
$$\therefore \quad -\frac{V_o}{R_F} = I_o e^{V_{in}/\eta V_T}$$

$$\therefore \quad V_o = -I_o R_F e^{V_{in}/\eta V_T}$$

- This equation shows that the output voltage Vo is proportional to the exponential function of V_{in}
- The exponential function is same as the antilog.

c) Draw and explain V to I converter with the grounded load.

Ans:- (Diagram- 2 mks, explanation/derivation 2 marks


R
V2
R
+Vcc
IB≅0
741
Io=Vin/R
IB≅0
-VEE
R
V1
I1
I2
Load
Vin.
IL

Analysis of the circuit: **(1M)**

- The analysis of the circuit can be done by following two steps: First step is to determine the voltage V_1 at the non- inverting (+) terminal and the second step is to establish relationship between V_1 and the load current I_L.
- Applying KCL at node V_1,

  $I_1 = I_1 + I_2$ ---------- (1)

  But $I_1 = V_{in} - V_1 / R$ and $I_2 = V_o - V_1 / R$, Substituting these expression into equation (1)

$$I_L = \frac{V_{in} - V_1}{R} + \frac{V_o - V_1}{R}$$

$$\therefore \quad V_{in} + V_o - 2V_1 = I_L R$$

$$\therefore \quad V_1 = \frac{V_{in} + V_o - I_L R}{2} \quad \text{-----(2)}$$

Thus we have obtained the expression for V1.

- The OP- AMP is connected in the non- inverting mode. Therefore gain of the circuit is,

$$A_{VF} = 1 + \frac{R}{R} = 2.$$

- The output voltage is given by,

$$V_o = A_{VF} \times V_1 = 2V_1$$

- Substituting V1 from equation (2) we get,

$$V_o = V_{in} + V_o - I_L R$$

$$\therefore \quad I_L R = V_{in}$$

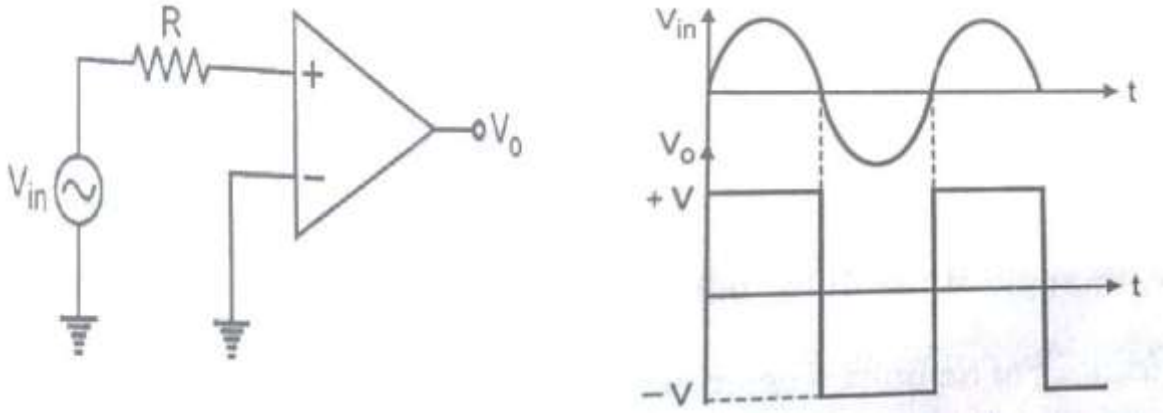
$$\therefore \quad I_L = \frac{V_{in}}{R} \quad \text{-----(3)}$$

- Equation 3 shows that the load current is dependent on the input voltage and resistor R. Note that all resistors in the figure must be equal in value.

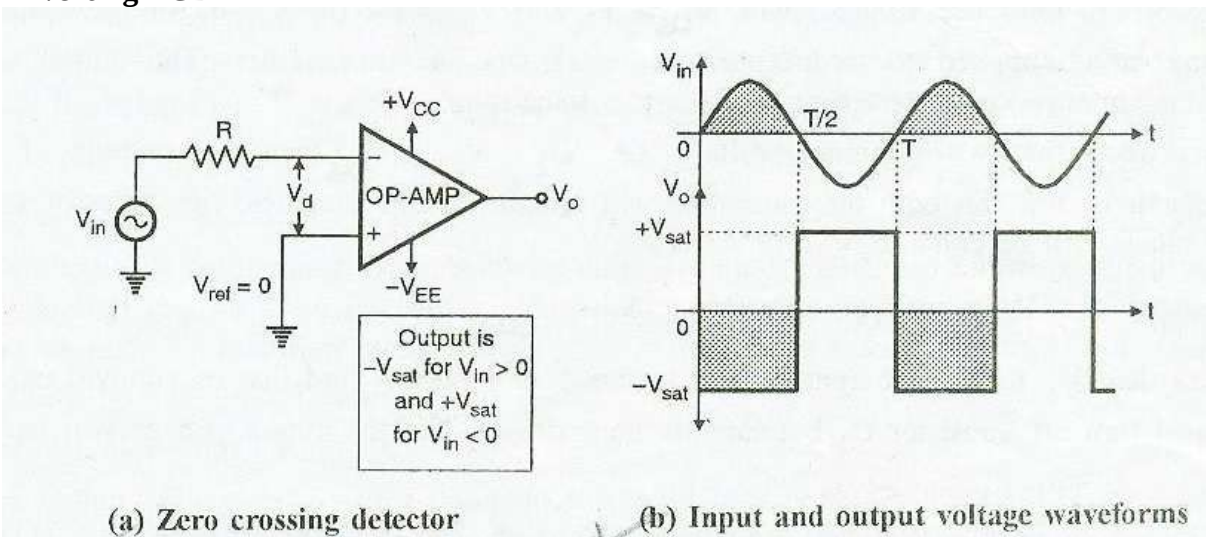
d) Draw circuit diagram and input-output waveforms of inverting ZCD and non-inverting ZCD(Zero crossing detector)

Ans: ***(1 mark for circuit diagram and 1 mark for waveform of inverting ZCD) & (1 mark for circuit and 1 mark for waveform of Non inverting ZCD)***

Non-inverting ZCD



Inverting ZCD



(a) Zero crossing detector (b) Input and output voltage waveforms

e) List any four advantages and four applications of instrumentation amplifier.

Ans: ***(2 marks - advantages & 2marks for applications)***

Advantages(Any 4)

1. Accurate Testing and Measurement
2. Stable and Easy to Use
3. Reliability of the Setup and Results
4. Highly Scalable

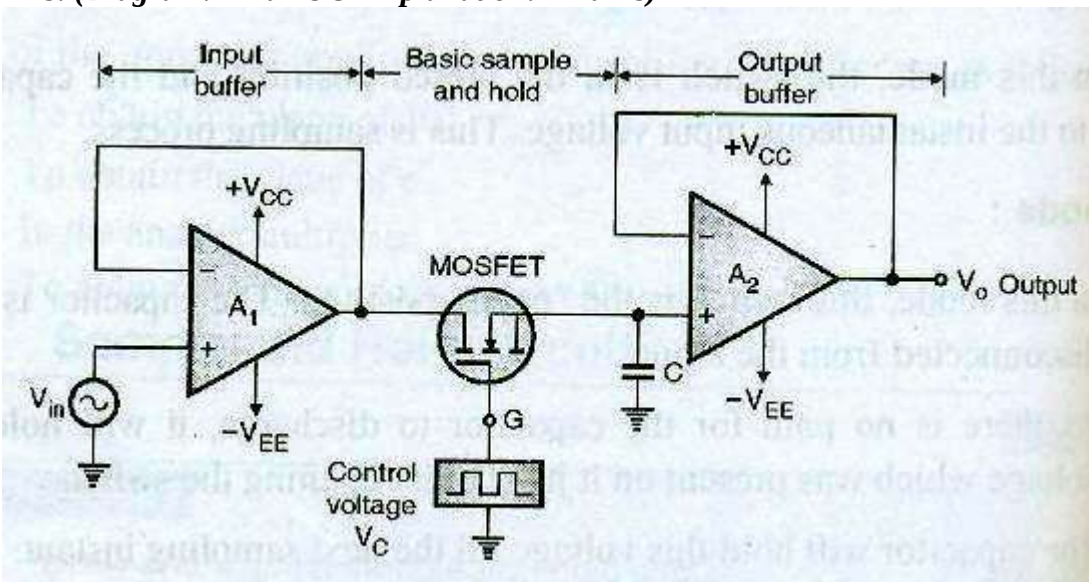
Applications (Any 4)

1) Electronic weighing scale
2) Temperature indicator
3) Temperature controller
4) Pressure monitoring and control
5) Light intensity meter

6) Measurement of flow and thermal conductivity

f) Draw and explain sample and hold circuit using op-amp.

Ans: ***(Diagram: 2Marks & Explanation: 2Marks)***



The n-channel MOSFET is driven by a control voltage VC acts as a switch.The control voltage VC is applied to the gate of the MOSFET.

The circuit diagram can be split into three stages. First stage is the voltage follower second one is the switch and capacitor and the third one is a gain the voltage follower.

When VC is high the MOSFET turns on and acts like a closed switch .This is sampling mode .The capacitor charges through the MOSFET to the instantaneous input voltage.

As soon as VC=0 the MOSFET turns off and the capacitor is disconnected from OPMP1output. Capacitor cannot discharge through amplifier A2 due to its high impedance. Thus this is the hold mode in which the capacitor holds the latest sample value.

The time period during which the voltage across capacitor is equal to input voltage is called sample period.

The time period during which the voltage across capacitor is constant is called Hold period.

4. Attempt any FOUR of the following:

a) Give classification of filters on the basis of –

i) Components used

ii) Frequency range

iii) Frequency response

iv) Nature of passband and stopband

Ans: ***(each correct classification – 1 mark)***

i. On the basis of component used, filters can be divided as active and passive filters.

ii. On the basis of frequency range, can be divided as AF (audio frequency) or RF (radio frequency) filters.

iii. On the basis of frequency response filters can be divided as high pass, low pass, band pass and band reject filters.

iv. On the basis of nature of pass band and stop band, they can be divided as narrow band pass, wide band pass, narrow band reject and wide band reject filters.

b) Design second order low pass filter to get pass band gain two and cut off frequency 1 KHz.

Ans:- (Correct design-3M, Designed circuit -1M)

Given:- Passband gain Af=2

Cut off frequency Fc = 1Khz

Pass band Gain (A_f) is given by the formula

$$A_f = 1 + \frac{R_f}{R_1}$$

Here, $A_f = 2$

Therefore, $2 = 1 + \frac{R_f}{R_1}$

So, $1 = \frac{R_f}{R_1}$

Therefore, $R_f = R_1$

Let $R_f = 10k\Omega$

Therefore, $R_1 = 10k\Omega$

Assume C = 0.01uF

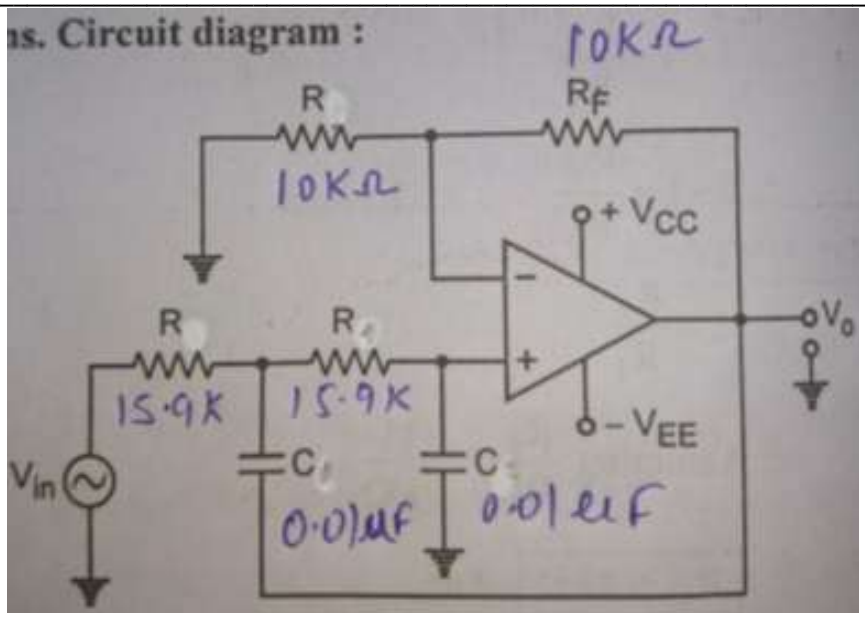
But $f_c = \frac{1}{2\pi RC}$

Given- Fc=1Khz

$1000 = 1/(2 * \pi * R * 0.01 * 10^{-6})$

R= 15.91 KΩ

The designed circuit is



c) Draw the circuit of wide band pass filter. Draw its frequency response characteristics.

Ans: (Diagram-2M, Frequency response-2M)

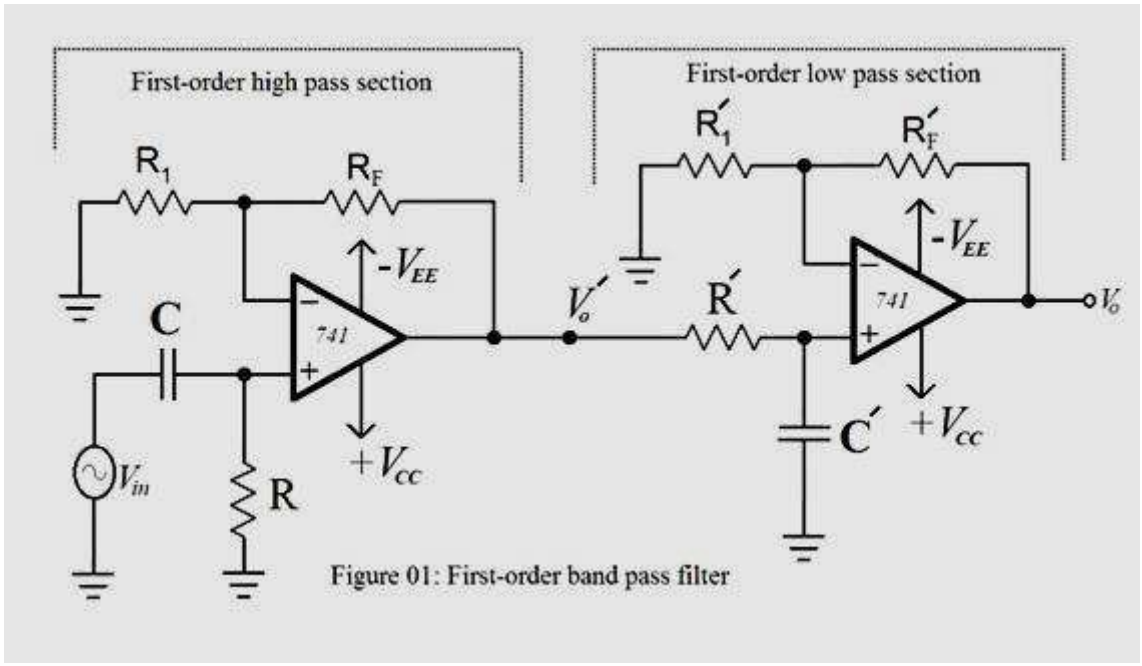
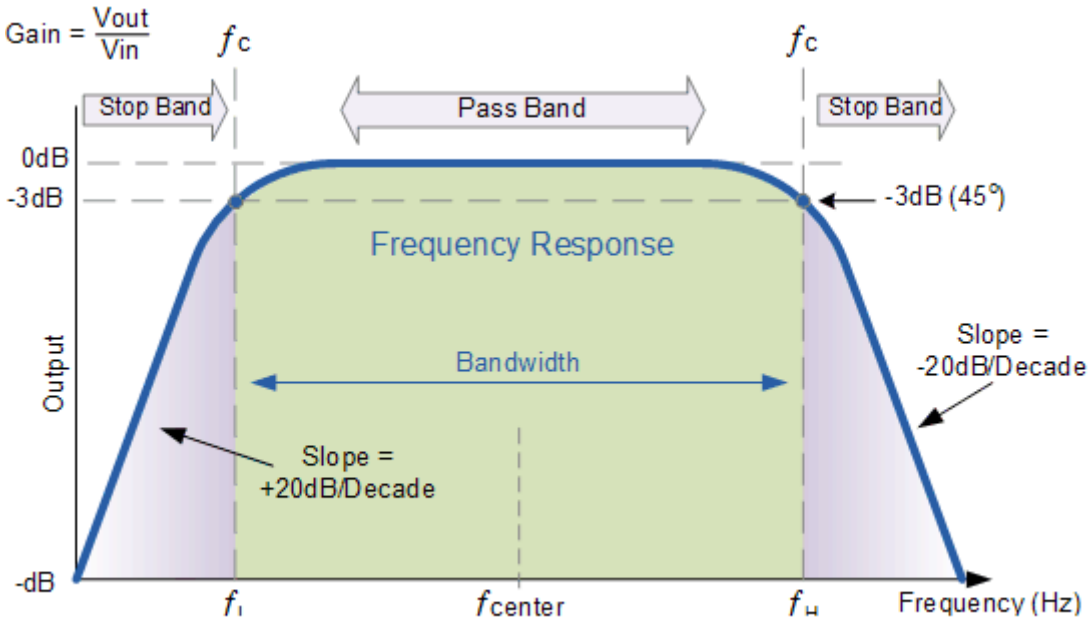
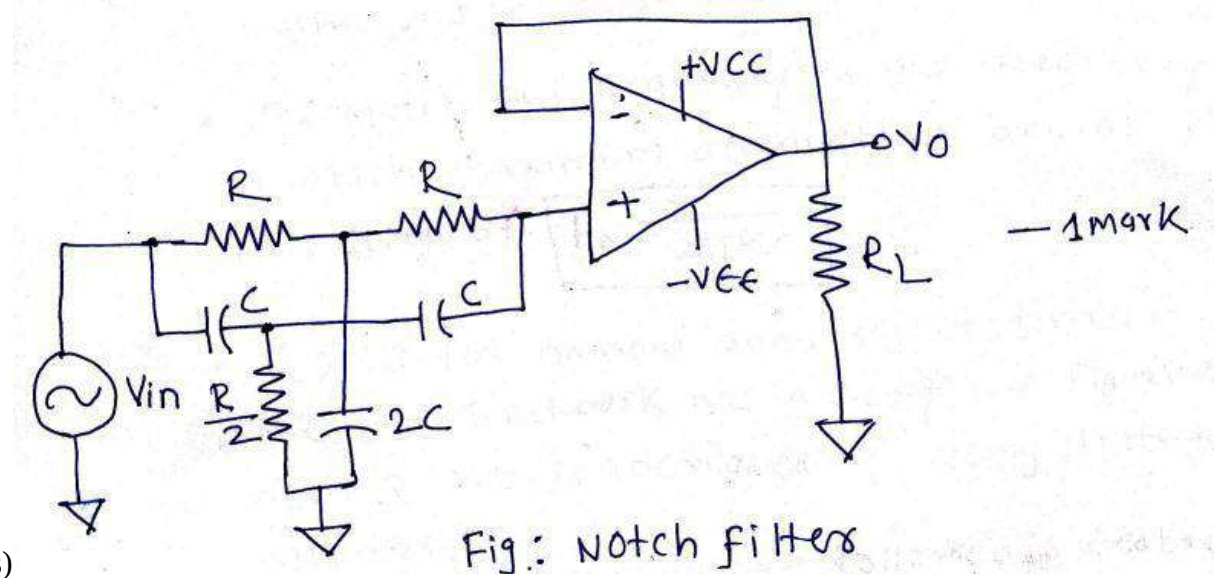


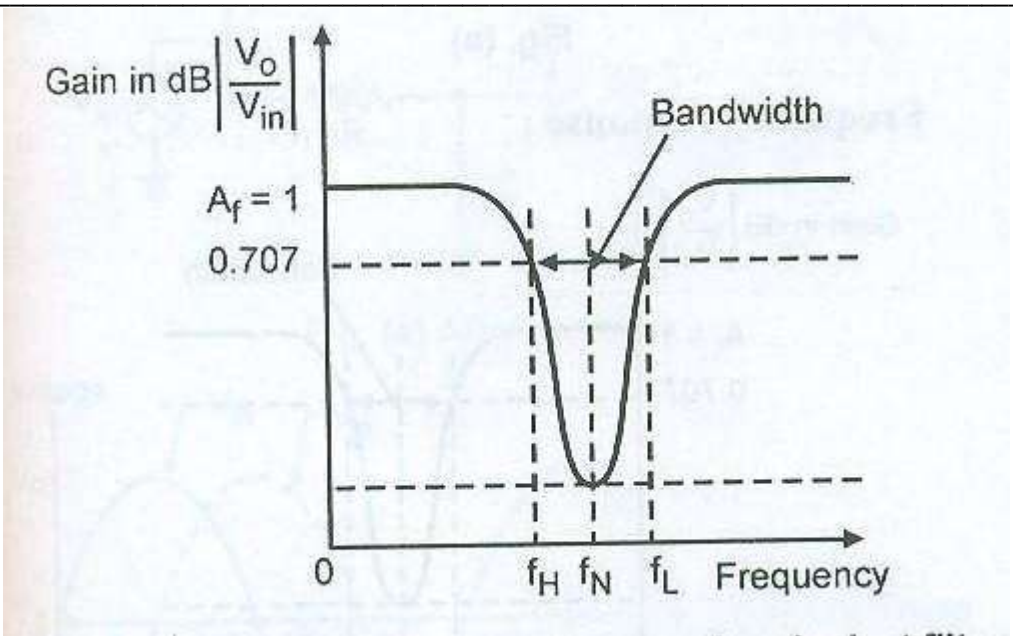
Figure 01: First-order band pass filter



d) Draw notch filter. Explain with characteristics.

Ans:- (Diagram – 2 mks, characteristics- 1 mks, explanation- 1 mks)





Characteristics-As seen from the characteristics-The notch filter has very narrow band rejection which depends on the value of Quality factor Q. Higher the value of Q, narrower is the band rejection .

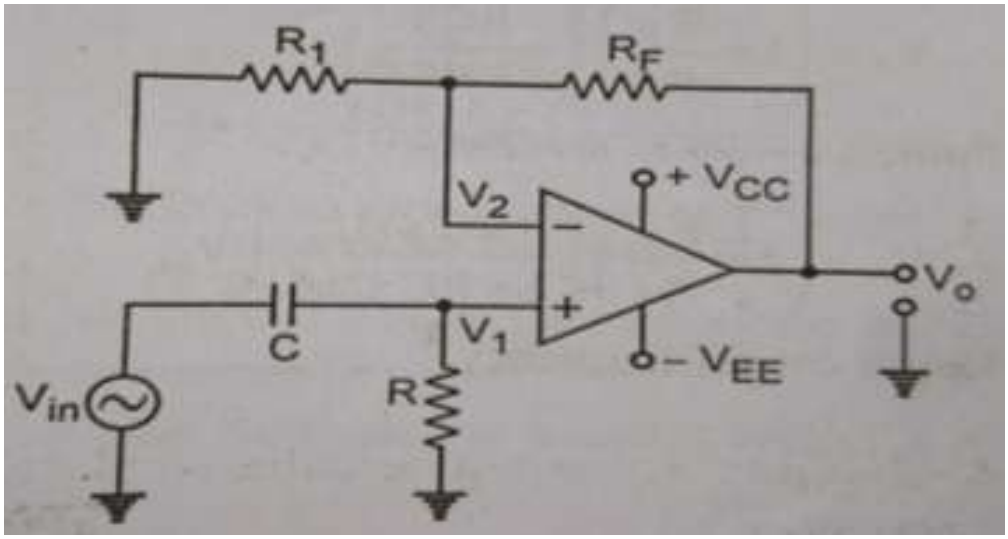
The Notch out frequency is the frequency at which maximum attenuation occurs. It is given by

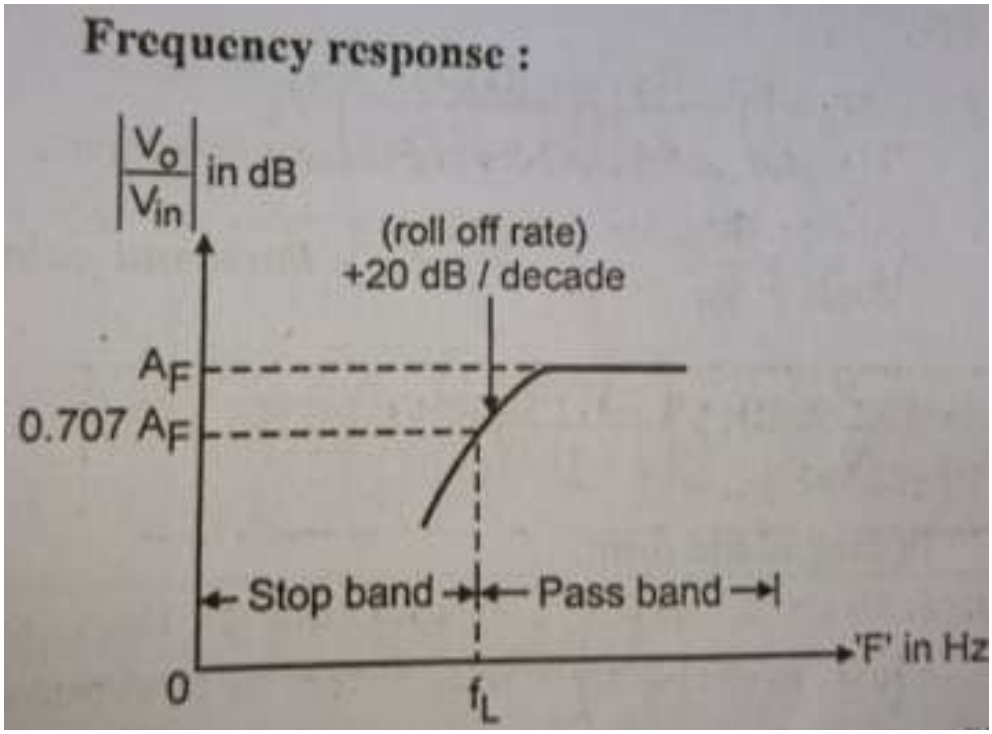
$$F_N = \frac{1}{2\pi RC}$$

Q > 10 narrow band reject filter.

e) Draw first order high pass filter and explain with characteristics.

Ans:- (Diagram- 2 mks, characteristics- 1 mks, explanation- 1 mks)





A high pass filter is one that passes the high frequency components and blocks the low frequency at a cut off frequency FL as shown in the characteristics below. The cut off frequency separates the pass band and the stop band. After FL, the gain increases at the rate of
+20 dB per decade increase in frequency.

f) Explain why active filter is better than passive filter.

Ans:-(Any four relevant points- 4 mks)

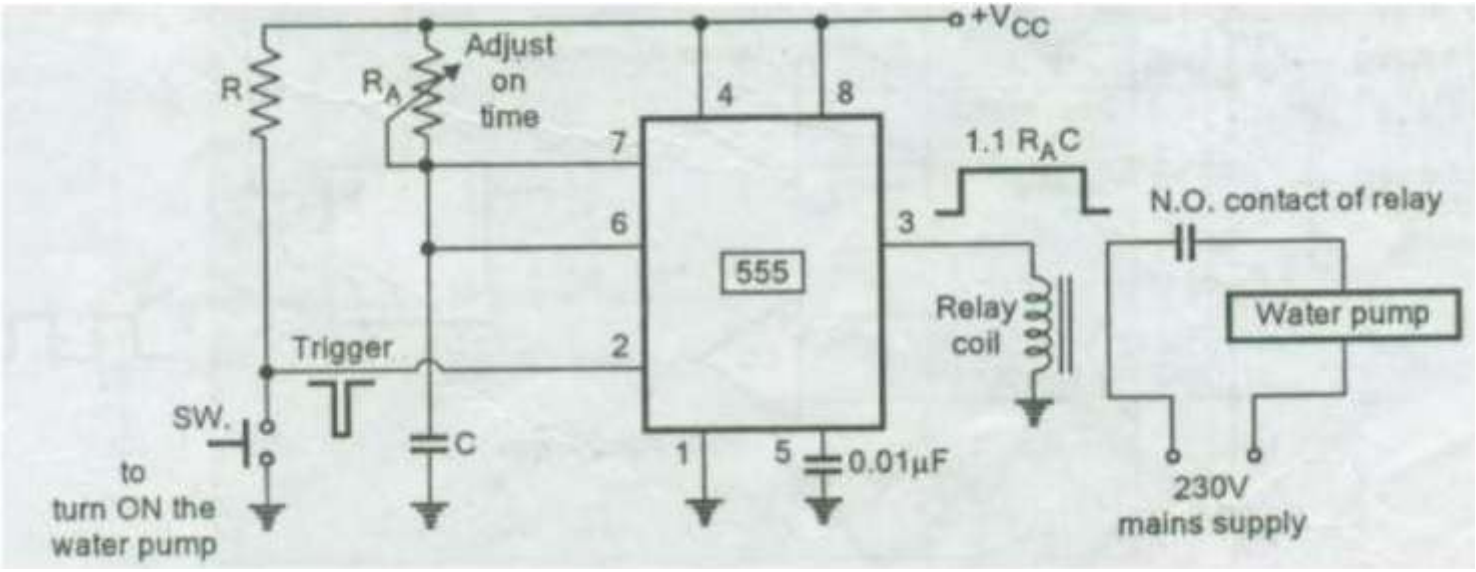
Advantages of active filters over passive filters

1. Active filters have flexibility in gain and frequency adjustments
2. They provide pass band gain
3. Because of high input resistance and low output resistance ,they do not have loading problems
4. The components required for active filters are of smaller size
5. They do not exhibit any insertion loss
6. Due to absence of inductors and easy availability of variety of cheaper op-amps active filters are cheaper
7. They allow for interstage isolation and control of input and output impedance

5. Attempt any FOUR of the following: 16

a) Draw and describe the operation of water level controller using IC555.

Ans:- Diagram- 2 mks, explanation-2 mks



Explanation-

IC 555 is used in the monostable multivibrator mode.

"SW" is a push to ON switch is used to turn on the timer and the water pump motor.

As soon as SW is switched this is used to turn on the timer and the water pump motor. IC 555, and output of 555 goes high.

It will remain high for period of $T_{on} = 1.1\ R_A C$. The high output of IC 555 will energize the relay coil, and close the N.O (normally open) contact of the relay to connect the 230 V ac supply to the water pump motor.

The pump motor will start and the water will be pumped into the overhead tank.

The motor will remain on for the ON time of the monostable circuit.

$T_{on} = 1.1\ R_A C$

The on time can be adjusted as per requirement by varying the resistance R_A.

b) Draw the block diagram of IC 555. State the function of both internal transistors in IC555.

Ans:-Block diagram- 2 mks, function of transistors- 1 mks each

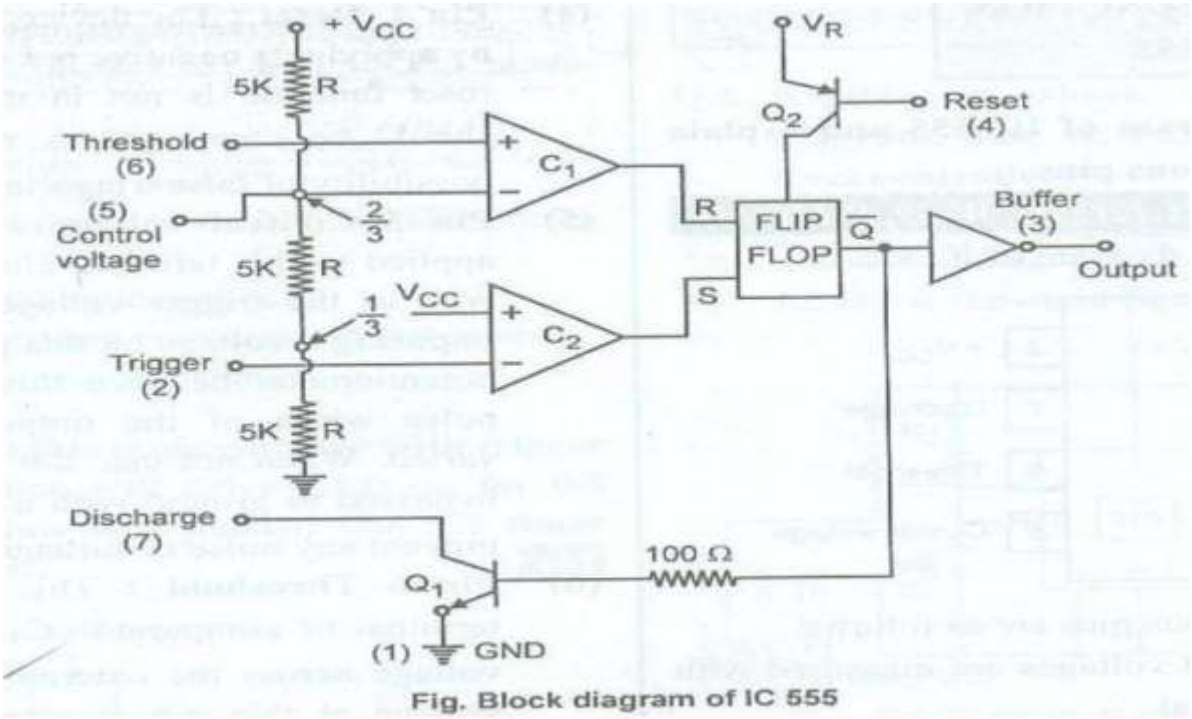


Fig. Block diagram of IC 555

Functions of internal transistors-

1. **Discharge NPN Transistor**-This transistor provides discharge path for external timing capacitor connected at pin no.7.

2**. Reset PNP Transistor**- an external negative trigger at base of reset transistor (pin no .4)

Will reset the IC timer 555. When not in use it is connected or shorted to +Vcc.

c) Describe with the help of block diagram, the operation of FM demodulator using PLL.

Ans :-Figure- 2Mks, Explanation-2Mks

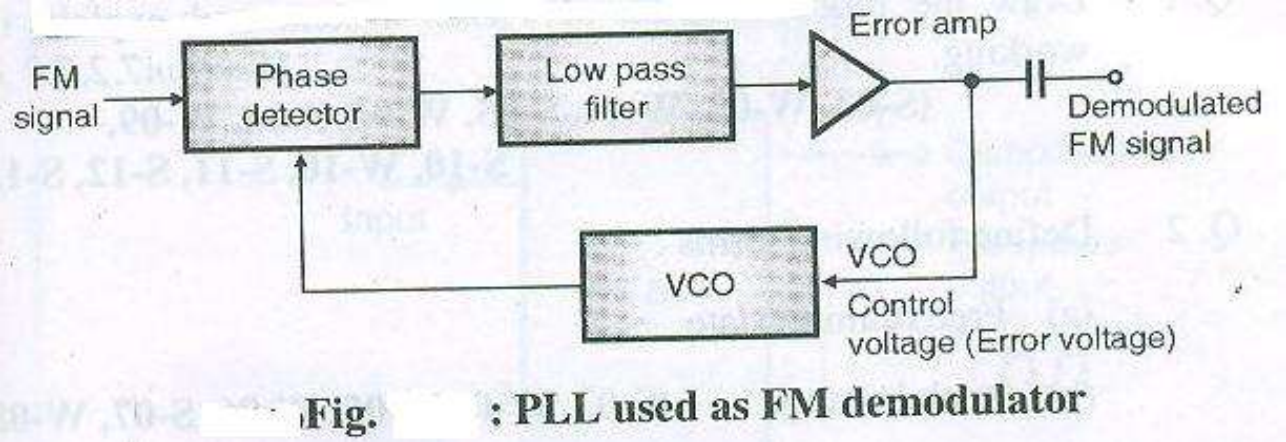
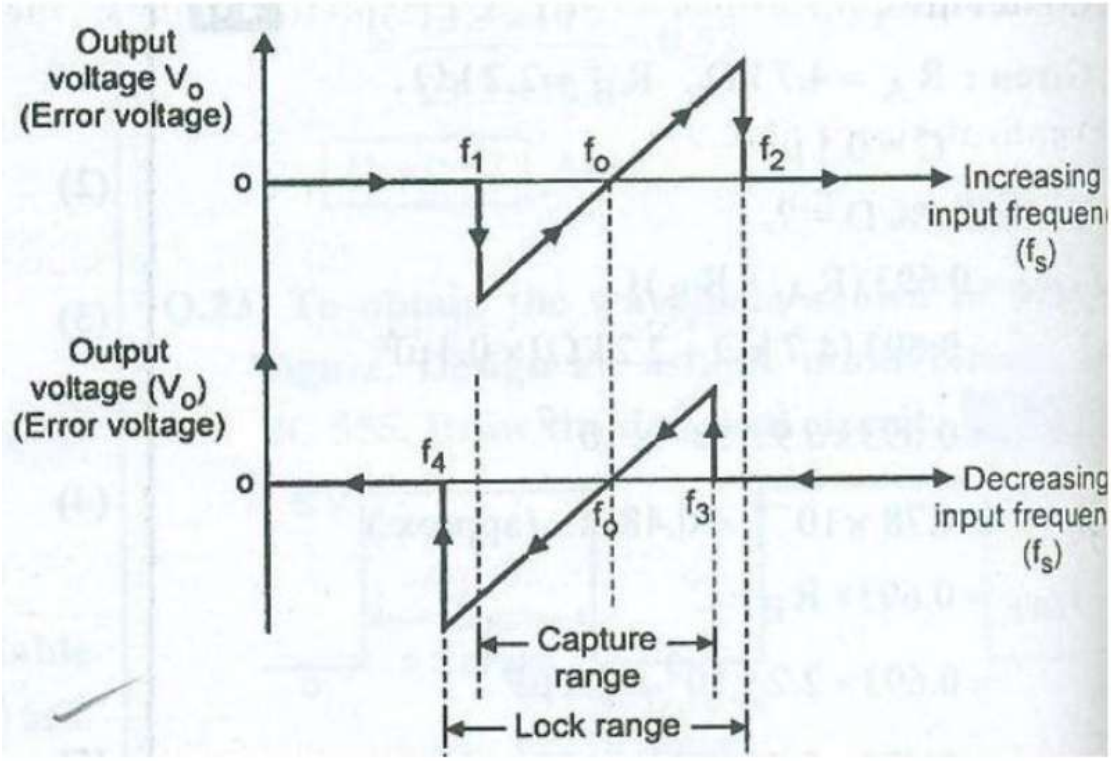


Fig. : PLL used as FM demodulator

Operation:
The FM signal which is to be demodulated is applied at the input of the PLL.As the PLL is locked to the FM signal, the VCO starts tracking the instantaneous frequency in the FM input signal.
The error voltage produced at the output of the amplifier is proportional to the deviation of input frequency from the center frequency of FM. Thus the ac component of the error voltage represents the modulating signal. Thus at the error amplifier output we get demodulated FM output.
The FM demodulator using PLL ensures a highly linear relationship between the instantaneous input frequency and VCO control voltage (error amplifier output)

d) Draw P.L.L. transfer curve. Explain – i) Capture range ii) Lock range.

Ans: (2 mks for transfer curve, 1 marks for lock range , 1 marks for capture range)



Transfer Curve

Lock range: the range of frequencies over which the PLL can maintain the phase lock with the incoming signal Fs, is defined as the lock in range.

Lock range = $f_L - 2 \Delta f_L$

Where $f_L = 8 f_0 / V$

Capture range : it is defined as the range of frequencies over which the PLL can acquire lock with the input signal Fs

Capture range = $2 \Delta f_c$

Where $f_c = f_L / (2\pi * 3.6 * 10^3 * C)$

e) Explain how mono-stable multi-vibrator can be used as frequency divider.

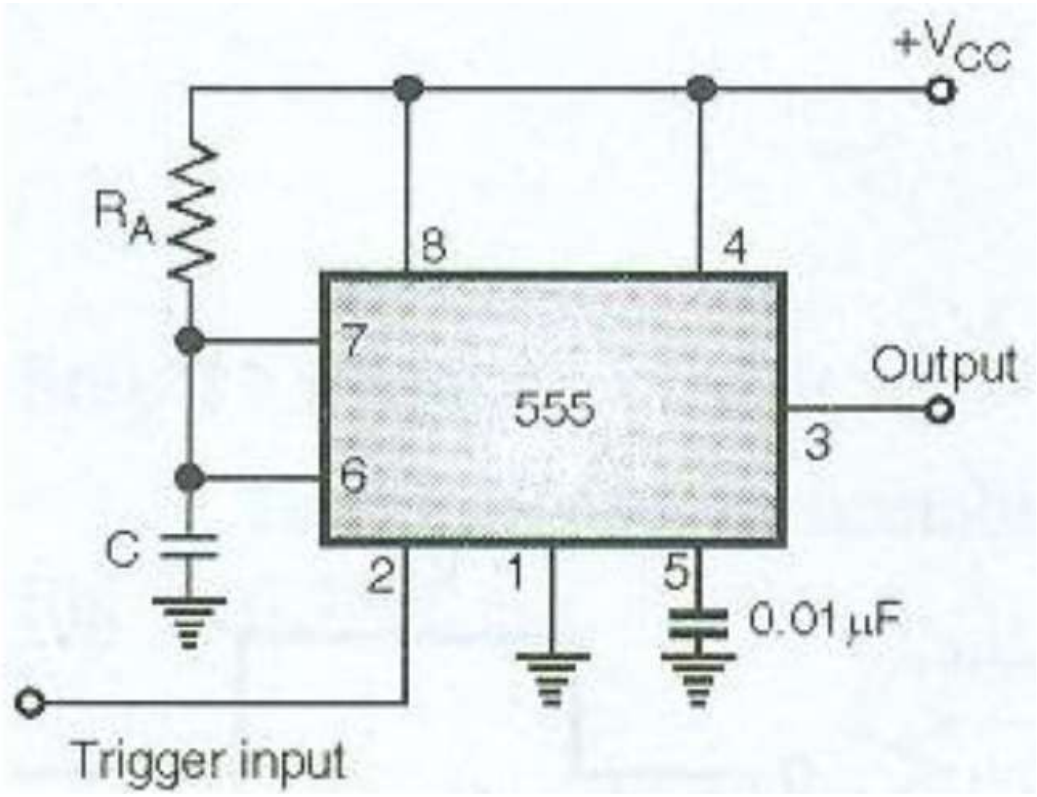
Ans:- Diagram – 2 mks, explanation- 1 mks, waveforms- 1 mks

Description-

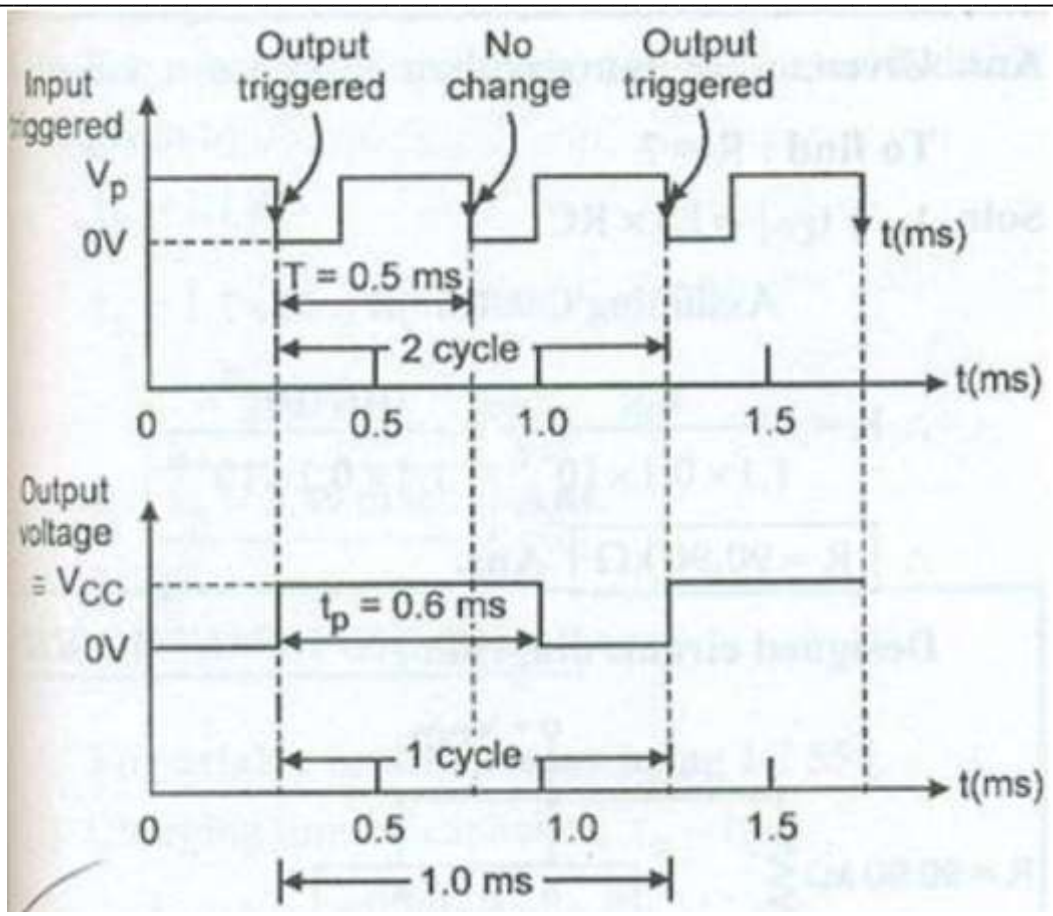
The monostable multivibrator can be used as frequency divider by adjusting the length of the timing cycle t_p with respect to time period T of the trigger input signal applied to pin 2.

To use the monostable multivibrator as divide by 2 circuit, the timing interval t_p must be slightly larger than the time period T of the trigger input signal as shown in figure below. By the same concept, to use the monostable multivibrator as divider by 3 circuit, t_p must be slightly larger than twice the period of the input trigger signal and so on.

The frequency divider application is possible because the monostable multivibrator cannot be triggered during the timing cycle.



Circuit Diagram



Waveforms as frequency divider

f) Draw and describe the operation of touch plate switch using IC555.

Ans: Circuit Diagram- 2Mks, Operation- 2Mks

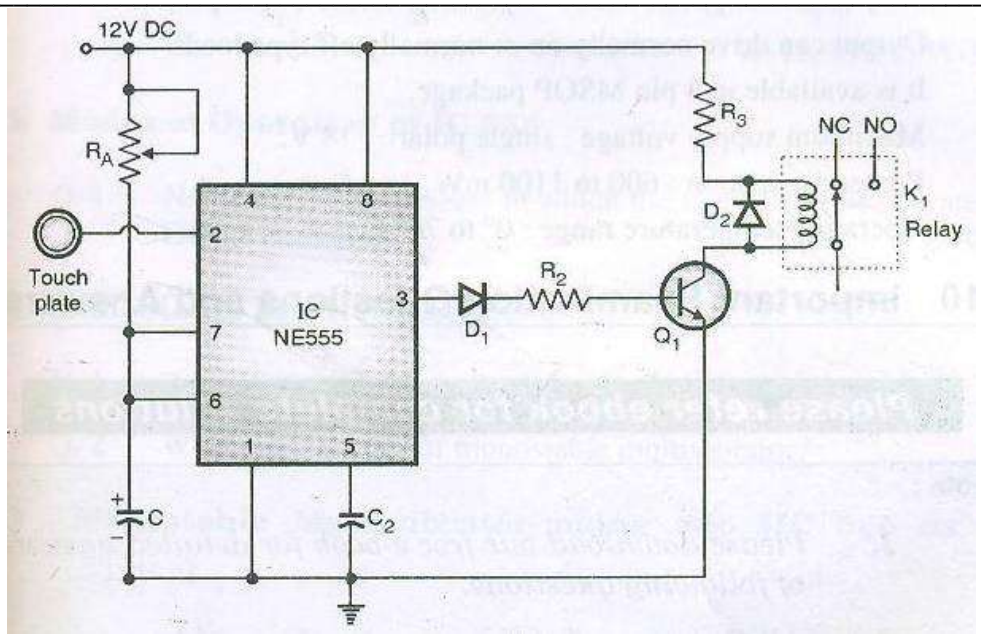


Fig: Touch switch circuit diagram

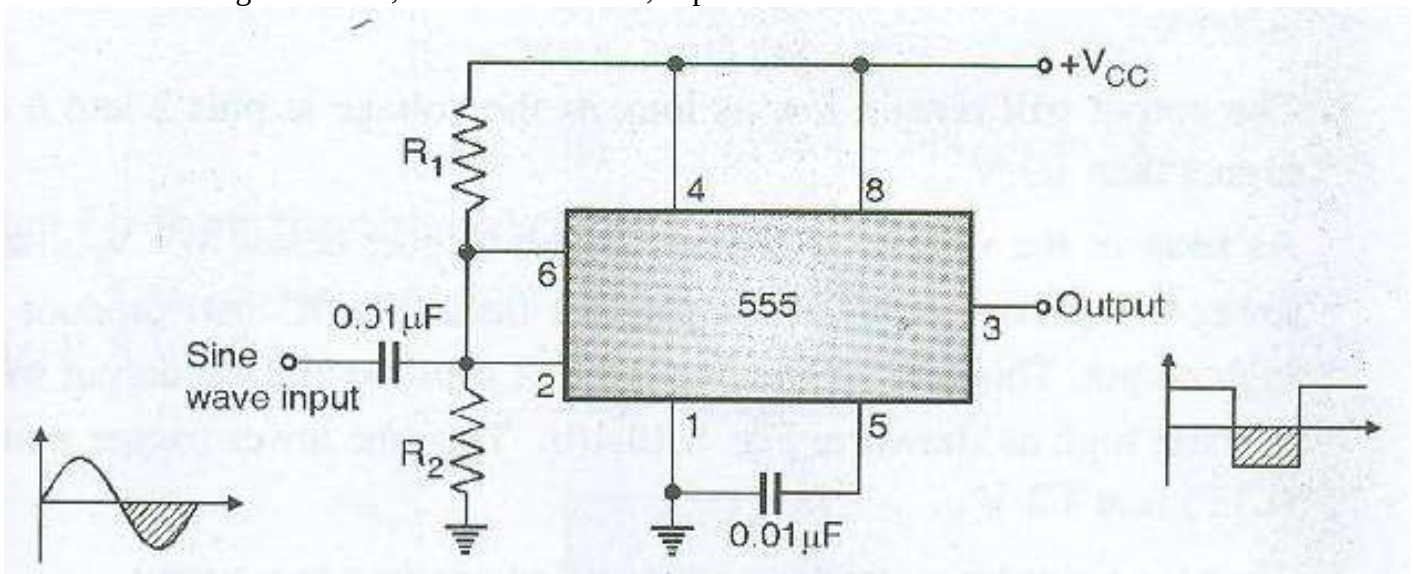
Operation: - A touch plate (push to ON) is used to turn on the timer and active the relay. As soon as touch plate is switched ON (pushed), a trigger pulse is produced and applied to pin no. 2 of IC 555, and the output of IC 555 goes high.

It will remain high for a period of TON= 1.1 RAC. The high output of IC 555 activates the transistor Q1 which in turn energize the relay coil, and closes the N.O (Normally open) contact of the relay.

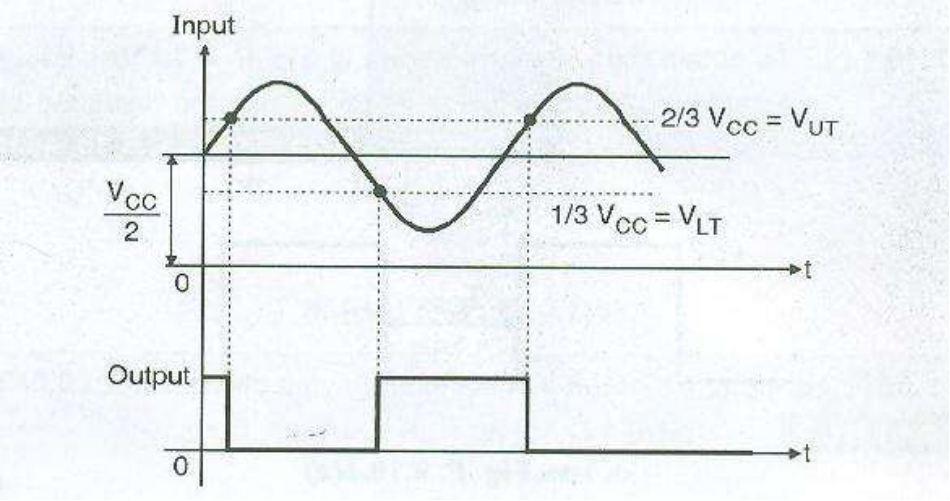
6. Attempt any FOUR of the following: 16

a) Explain the working of IC 555 as Schmitt trigger. Draw circuit diagram and output waveforms.

Ans :-. Circuit diagram: 2Mks, Waveforms: 1Mks, explanation-1 mks



Schmitt trigger using IC 555.



Waveforms of Schmitt trigger using IC 555

Explanation-

Pins 4 and 8 are connected to the supply (VCC). The pins 2 and 6 are tied together and the input is given to this common point through a capacitor C. this common point is supplied with an external bias voltage of VCC / 2 with the help of the voltage divider circuit formed by the resistors R1 and R2.The important characteristic of the Schmitt trigger is Hysteresis. The output of the Schmitt trigger is high if the input voltage is greater than the upper threshold value and the output of the Schmitt trigger is low if the input voltage is lower than the lower threshold value.The output retains its value when the input is between the two threshold values. The usage of two threshold values is called Hysteresis and the Schmitt trigger acts as a memory element (a bistable multivibrator or a flip-flop).The threshold values in this case are 2/3 VCC and 1/3 VCC i.e. the upper comparator trips at 2/3 VCC and the lower comparator trips at 1/3 VCC. The input voltage is compared to these threshold values by the individual comparators and the flip-flop is SET or RESET accordingly. Based on this the output becomes high or low.When a sine wave of amplitude greater than VCC / 6 is applied at the input, the flip-flop is set and reset alternately for the positive cycle and the negative cycle.

b) Draw and describe operation of Bistable multivibrator using op-amp.

Ans:- Diagram- 2 mks, explanation- 1 mks, waveforms- 1 mks

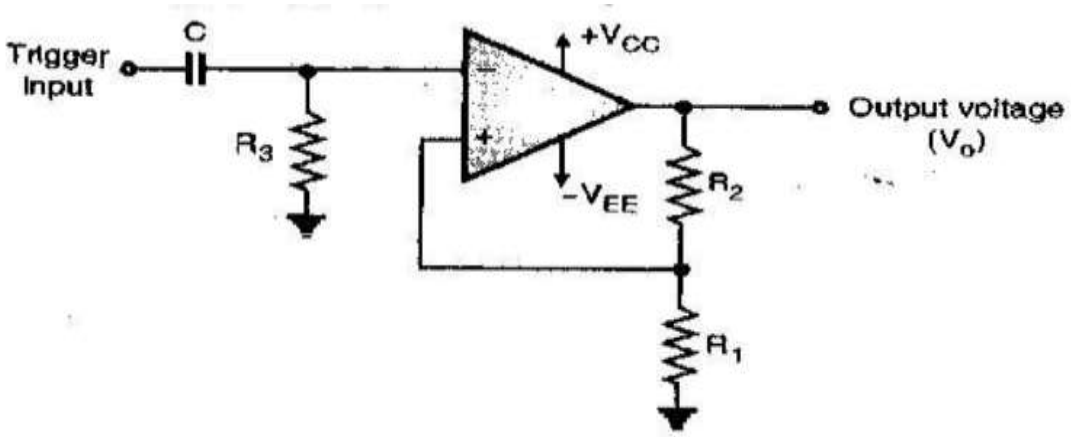
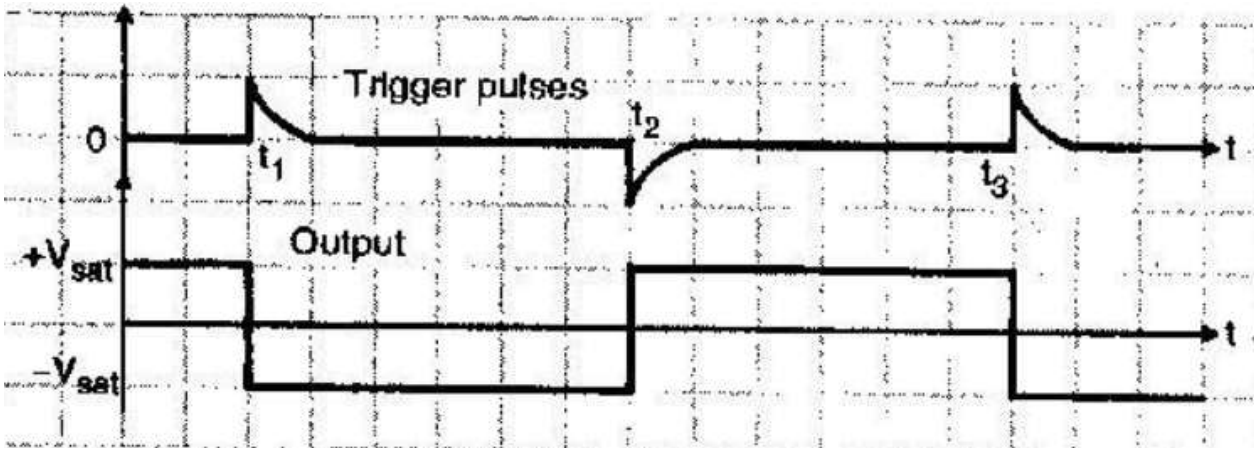


Fig. .(a) shows the circuit diagram of a bistable multivibrator using OP-AMP 741. This circuit will have two stable states.

In one stable state, the output voltage is + V_{sat} and in the other one it will be – V_{sat}. To switch over from one stable state to the other, we need to apply trigger pulses at the input.



Waveforms

Operation of the circuit :

- Initially assume that the output voltage is equal to + V_{sat}. Therefore voltage at the non-inverting terminal (+) is given by,

$$V_{NON-INV} = \frac{R_1}{(R_1 + R_2)} \times (+ V_{sat})$$

- The voltage at the inverting (–) terminal is given by,

$$V_{INV} = 0$$

This is because the inverting terminal is connected to ground through the resistor R_3. Output voltage $V_o = + V_{sat}$ is one stable state of the circuit.

In order to change the state of output from $+ V_{sat}$ to $- V_{sat}$, it is necessary to have a higher positive voltage at the inverting (–) terminal, than that of the non-inverting (+) terminal. Therefore we apply a positive pulse at instant "t_1" at the trigger input terminal, as shown in Fig. (b). The amplitude of trigger pulse is given by,

$$V_{TRIGGER} > \frac{R_1}{(R_1 + R_2)} \times (+ V_{sat})$$

As soon as this pulse is applied, the OP-AMP will change its output from $+ V_{sat}$ to $- V_{sat}$. This is the second stable state of this circuit.

In this stable state the voltage at non-inverting (+) terminal will be equal to,

$$V_{NON\text{-}INV} = \frac{R_1}{(R_1 + R_2)} \times (- V_{sat})$$

In order to switch the output from $- V_{sat}$ to $+ V_{sat}$, it is necessary to apply a negative trigger pulse at the input. The amplitude of this trigger pulse is given by,

$$V_{TRIGGER} = \frac{R_1}{(R_1 + R_2)} \times (- V_{sat})$$

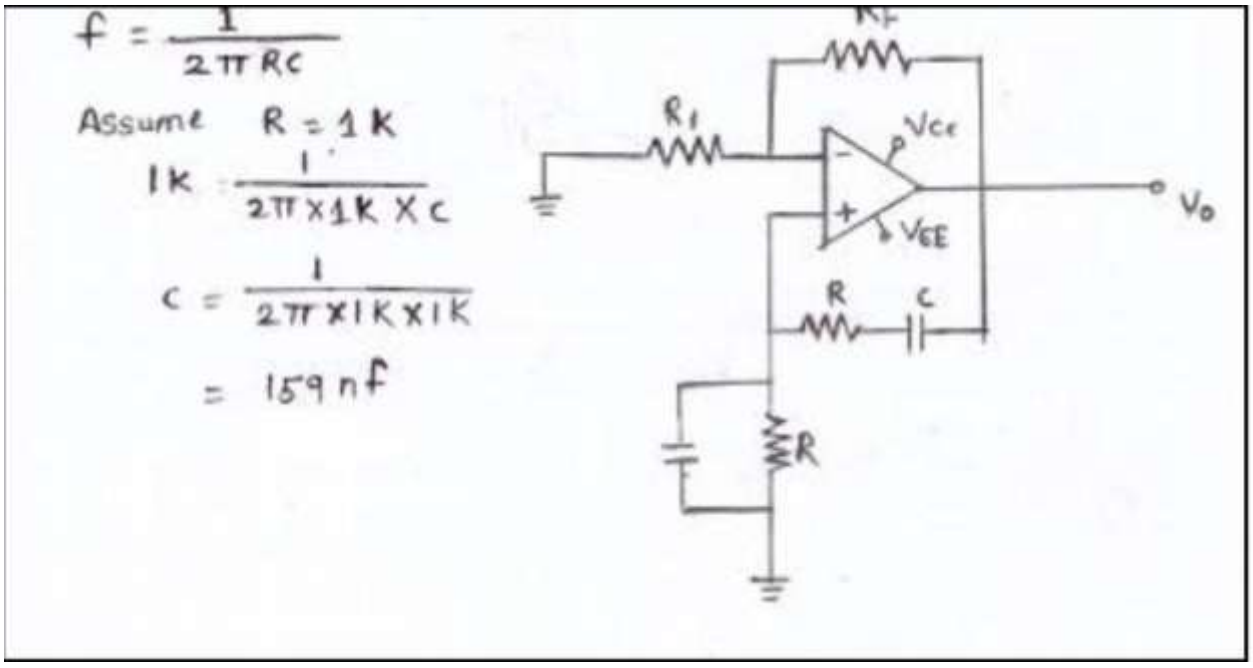
At the instant "t_2" as shown in Fig. (b), a negative trigger pulse of adequate amplitude is applied at the input of the circuit. The output will switch over from $- V_{sat}$ to $+ V_{sat}$ at this instant.

c) Design and draw op-amp based wein bridge oscillator for frequency 1 KHz.

Ans:- Proper design steps and values -2 mks, diagram- 2 mks

NOTE: students can assume any value of R so accordingly answer for C will change.

Let $R_1=R_F=1\ K\Omega$

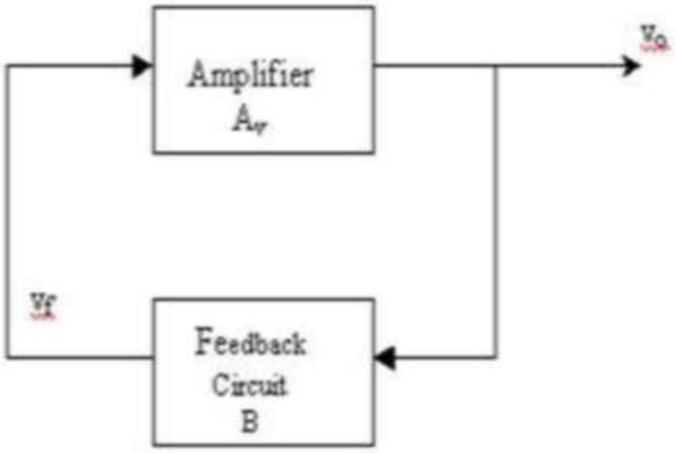


d) Explain principle of oscillator with block diagram.

Ans: -Block diagram- 2 mks, principle – 2 mks

An electronic **oscillator** is an electronic circuit that produces a periodic, oscillating electronic signal, often a sine wave or a square wave. **Oscillators** convert direct current (DC) from a power supply to an alternating current (AC) signal and works with positive feedback principle.

$$\frac{v_o}{v_i} = \frac{A_v}{1 - A_v B}$$



$v_{in} = 0$ and $v_o \neq 0$ implies that

- $A_v B = 1$
- Expressed in polar form,
- $A_v B = 1 \angle 0^0$

In order to satisfy the above criterion, the oscillator must be able to achieve positive feedback at some frequency w_0 where the magnitude of the loop gain is exactly unity. <**Barkhausen Criterion**>

e) Give advantages and disadvantages of wein bridge oscillator.

Ans:- 2 mks for 2 advantages, 2 mks for 2 disadvantages

Advantages-

1) Suitable for low frequency oscillations

2) simple circuit and frequency can be easily adjusted.

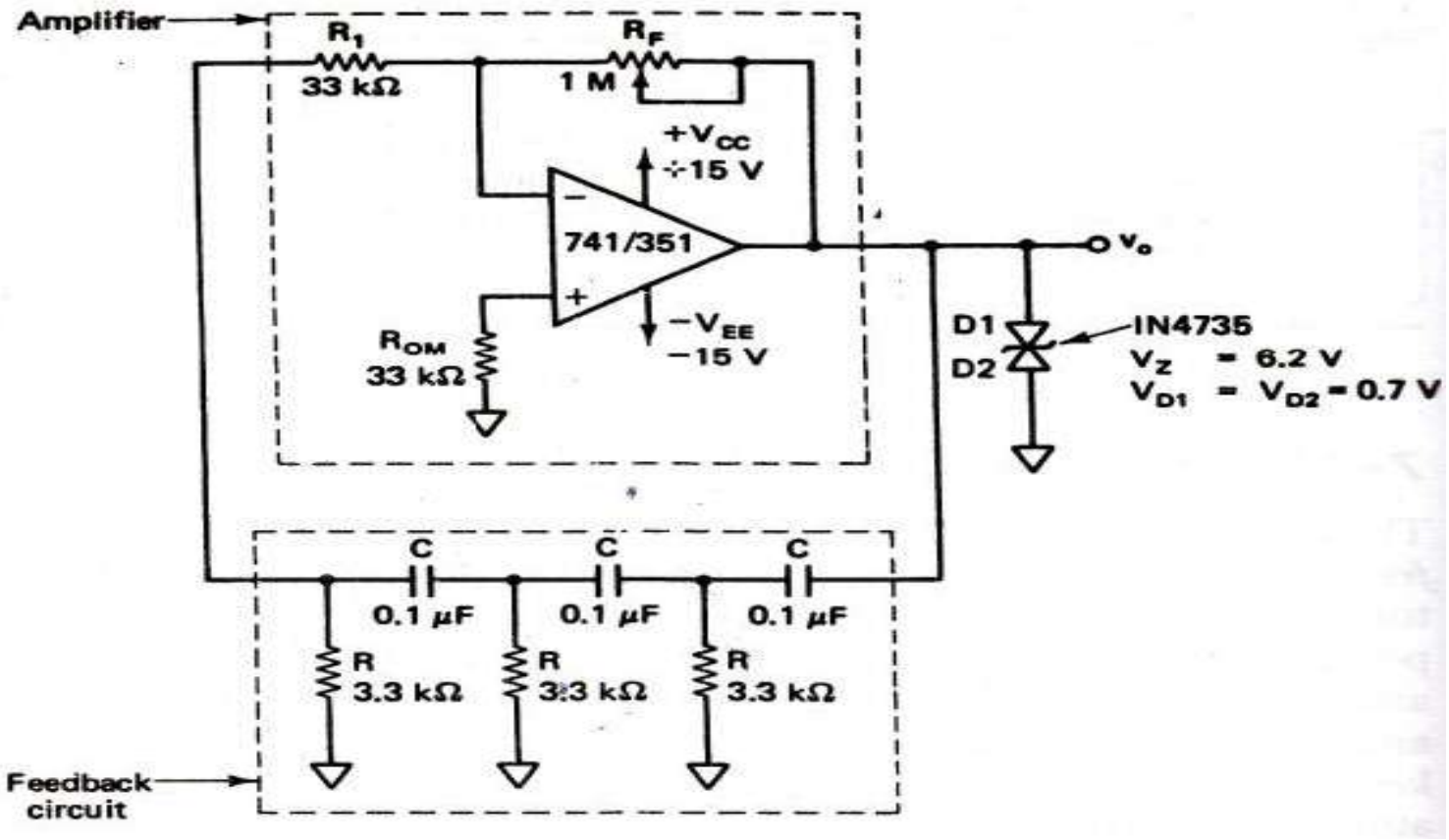
Disadvantages

1) Not suitable for high frequency applications

2) Problem of frequency unstability.

f) Draw the circuit diagram of phase shift oscillator using IC-741. State any two applications of it.

Ans: Diagram. – 2mks, 2 applications -2 mks



Applications: RC Phase Shift Oscillators are used in musical instruments, voice synthesis and in GPS units since they work at all audio frequencies.