11819

17659

3 Hours / 100 Marks Seat No. | | | | | | | | |

Instructions : *(1)* ***All*** *questions are* ***compulsory****.*
(2) Answer ***each*** *next main question on a* ***new*** *page.*
(3) Illustrate your answers with neat sketches ***wherever*** *necessary.*
(4) Figures to the ***right*** *indicate* ***full*** *marks.*
(5) Assume suitable data, if ***necessary****.*

Marks

1. A) Attempt **any three** : **(3×4=12)**

1) Compare Asynchronous sequential and synchronous sequential circuits.
2) Explain estimation of channel capacitance of CMOS.
3) Draw CMOS two input NOR gate and write it's truth table.
4) State any 4 features of VHDL.

B) Attempt **any one** : **(1×6=6)**

1) Compare FPGA and CPLD (any six pts.)
2) State any one process for wafer fabrication with diagram.

2. Attempt **any four** : **(4×4=16)**

1) Explain fabrication using N-well process.
2) Design $Y = \overline{AB}.\ \overline{CD}$ using CMOS logic.
3) What do you mean by simulation ? Why it is necessary ?
4) Compare Mealy M/C with Moore M/C.
5) Write VHDL code for half adder.

3. Attempt **any four** : **(4×4=16)**

1) Write the syntax of entity and architecture used in VHDL and explain it.
2) Draw 2 : 4 decoder and write VHDL code for it.
3) Describe Twin-tube process with diagram.
4) What do you meant by sensitivity list and zero modeling ?
5) Compare signals and variables in VHDL.

P.T.O.

Marks

4. A) Attempt **any three** : **(3×4=12)**

1) Define the following terms :
   i) Noise margin
   ii) Power fanout
   iii) Skew
   iv) Meta stability
2) Explain event scheduling with suitable example.
3) What is test bench ? Write its applications.
4) List different concurrent statements and give the example of any two.

B) Attempt **any one** : **(1×6=6)**

1) Draw architecture of XC9500 CPLD.
2) Design a sequence detector to detect the sequence 110. Use D F/F to design the circuit.

5. Attempt **any four** : **(4×4=16)**

1) Draw the HDL design flow for synthesis.
2) State the function of each step elements of VHDL.
3) Draw CMOS inverter characteristic and explain it.
4) Write VHDL code for 4 : 1 MUX.
5) List the types of FSM. Draw labelled diagram of each.

6. Attempt **any four** : **(4×4=16)**

1) Explain basic architecture of Spaston-3 FPGA series.
2) Write VHDL code for 3-bit down counter.
3) Draw design flow of ASIC and explain it.
4) Explain the shift and logical operations.
5) State different modeling styles used in VHDL and write VHDL code for 1 : 4 DEMUX using any one style.
