Important Instructions to examiners:

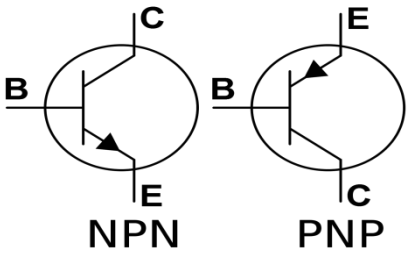
1) The answers should be examined by key words and not as word-to-word as given in the Model answer scheme.
2) The model answer and the answer written by candidate may vary but the examiner may try To assess the understanding level of the candidate.
3) The language errors such as grammatical, spelling errors should not be given more Importance (Not applicable for subject English and Communication Skills.
4) While assessing figures, examiner may give credit for principal components indicated in the Figure. The figures drawn by candidate and model answer may vary. The examiner may give credit for any Equivalent figure drawn.
5) Credits may be given step wise for numerical problems. In some cases, the assumed constant Values may vary and there may be some difference in the candidate's answers and model answer.
6) In case of some questions credit may be given by judgment on part of examiner of relevant answer based on candidate's understanding.
7) For programming language papers, credit may be given to any other program based on equivalent concept.

Q1.A) Attempt any Six: **12 M**

a) Draw the symbol of NPN and PNP BJT.

Ans:

Symbol Of NPN and PNP BJT **01M each**



b) State two advantage of voltage divider biasing technique.

Ans:

Advantages:- **01M each**

1. Excellent Stabilization is provided by R_E.
2. Smallest possible value of "S" leads to the max. Possible thermal stability.

c) State two applications of direct coupling method used in multistage amplifier.(any two)

Ans:

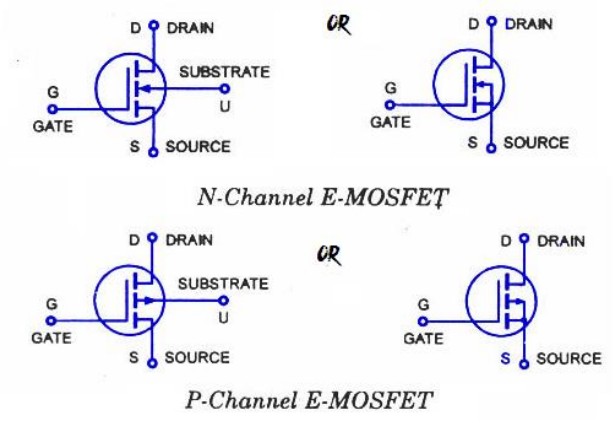
Applications (any two) **01M each**

1. Low frequency Analog computation.
2. Power supply regulators.
3. Bioelectric measurements.
4. For amplifying extremely low frequency signals.

d) Draw the symbols enhancement p type and enhancement n type MOSFET

Ans

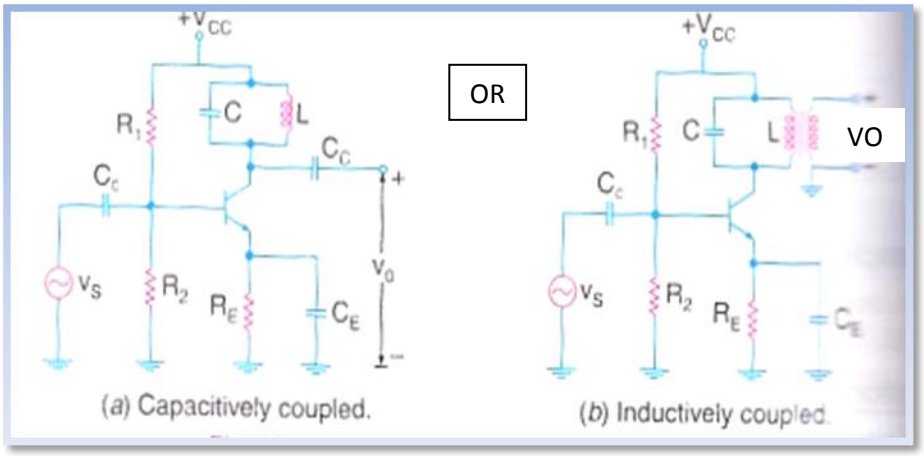
Symbol enhancement p type and enhancement n type MOSFET **01Meach**



e) Sketch the circuit diagram of single tuned amplifier.

Ans:

Diagram:- **02M**



f) State the maximum efficiency of class A power amplifier.

Ans: **02M**

The maximum possible overall efficiency of a class A amplifier is 25%.

OR

The maximum possible value of collector efficiency of a class A amplifiers 50%.

g) State two advantage of JFET over BJT.

Ans:

Advantages of JFET over BJT (any four) **1/2M each**

i) It is less noisy than BJT
ii) high input impedance
iii) low power consumption
iv) No thermal Runaway occurs in FET.
v) It is used in High frequency applications.
v) It is unipolar Device.

h) Define intrinsic stand-off ratio ηof UJT.

Ans:

Intrinsic Stand-Off Ratio:-

(η) is defined as the ratio of R_{B1} and $R_{BB.}$ **01M**

Where

R_{B1} is the resistance between emitter and base 1

R_{BB} is the resistance between base1and base2 ($R_{BB} = R_{B1} + R_{B2}$)

$$\eta = \frac{R_{B_1}}{R_{BB}} = \frac{R_{B_1}}{R_{B_1}+R_{B_2}}$$ **01M**

Q1. B) Attempt any two: **08M**

a) Compare CB, CE and CC with respect to Input impedance, output impedance, current gain and voltage gain. Give typical figures of each parameter

Ans:- **01Mark each**

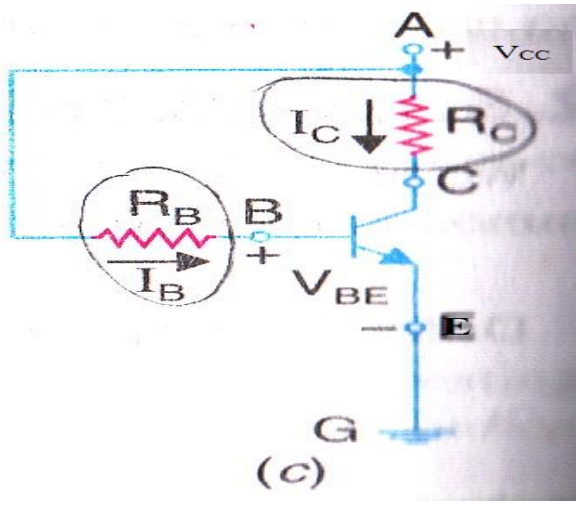
Note: - (Values may differ since different reference books provide different values)

Parameters	CB	CE	CC
Input Impedance	Low(100Ω)	Low(750Ω)	Very High(750KΩ)
Output Impedance	Very High(450KΩ)	High(45kΩ)	Low(50Ω)
Current Gain	Less than unity	High (100)	High(100)
Voltage Gain	High(About150)	Very high(about 500)	Less than 1

b) Draw the circuit diagram and explain the operation of fixed biasing circuit used in BJT. State its advantages and disadvantages.

Ans:-

Circuit diagram:- **01M**



Explanation:- **01M**

The above equation gives the voltage drop across the collector emitter terminals of transistor . The value of collector current is given by the relation.

$$I_C = \beta \frac{V_{CC}}{R_B} = \frac{V_{CC}}{R_B/\beta}$$

The above relation shows that the collector current is β times greater than the base current and is not at all dependent on the resistance of the collector circuit.

It may be noted from the equations that the values of collector current (I_C) and collector-to emitter voltage (V_{CE}) are dependent on β. But β is strongly dependent upon temperature. It means that collector current and collector – to emitter voltage of a bias circuit (which sets the Q-points of a transistor) will vary with the change in value of b due to variation in temperature. It means that it is impossible to obtain a stable Q-point in a base –bias circuit. Because of this fact, the base bias is never used in amplifier circuits.

Advantage:- **01M**

- The fixed bias circuit is simple and has less number of components
- It gives very good flexibility as the Q-point can be set at any point in the active region by adjusting the value of R_B.

Disadvantage:- **01M**

- Very poor thermal stability as
  $S = (1 + \beta)$
- With change in β due to changes in temp., the operating point keeps on shifting its position.

c) With the help of neat circuit diagram and V-I characteristic explain the working of zener diode as voltage regulator.

Ans:

Working of Zener Diode as Voltage Regulator:- **03M**

i] REGULATION BY VARYING INPUT VOLTAGE :-

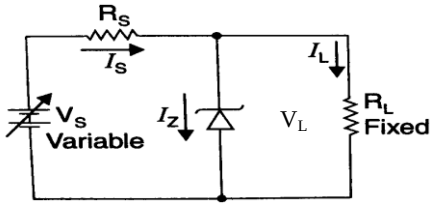
A resistance (Rs) is connected in series with the zener diode to limit current in the circuit. For proper operation, the input voltage (Vs) must be greater than the zener voltage (Vz).

$$V_L = V_Z + I_Z . R_Z$$

Where,
Rz= zener resistance

$$I_L = \frac{V_L}{R_L}$$

$Is = Iz + I_L$



(a) Varying input voltage.

Here the load Resistance is kept fixed and input voltage is varied within the limits

CONDITION 1:- WHEN INPUT VOLTAGE IS INCREASED

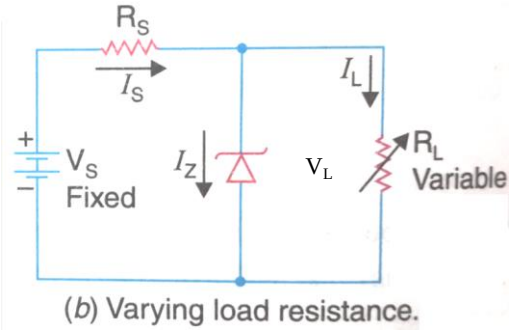
When input voltage is increased the input current (Is) also increases. Thus current through zener diode gets increased without affecting the load current(IL).The increase in input voltage also increases the voltage drop across the resistance Rs thereby keeping the VL constant.

CONDITION 2:- WHEN INPUT VOLTAGE IS DECREASED

When input voltage is decreased, the input current gets reduced, as a result of this Iz also decreases. The voltage drop across Rs will be reduced and thus the load voltage (V_L) and load current (I_L) remains constant.

OR

ii] REGULATION BY VARYING LOAD RESISTANCE:- **03M**



(b) Varying load resistance.

In this method the input voltage is kept constant whereas load resistance R_L is varied.

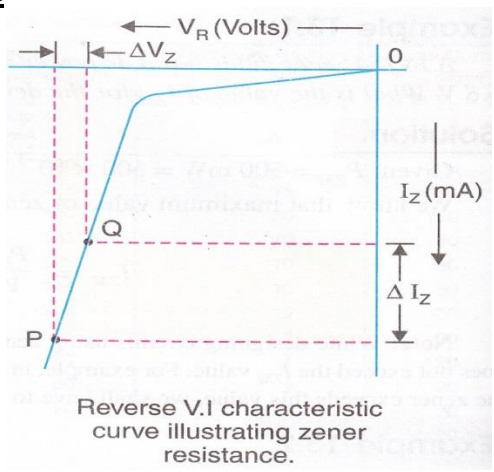
CONDITION 1:- WHEN **LOAD RESISTANCE IS INCREASED**

When load resistance is increased, the load current reduces, due to which the zener current I_Z increases. Thus the value of input current and voltage drop across series resistance is kept constant. Hence the load voltage remains constant.

CONDITION 2:- WHEN LOAD RESISTANCE IS REDUCED

When load resistance is decreased, the load current increases. This leads to decrease in I_Z. Because of this the input current and the voltage drop across series resistance remains constant. Hence the load voltage is also kept constant.

Characteristics of Zener Diode **01M**



Reverse V.I characteristic curve illustrating zener resistance.

Q2) Attempt any four: **16M**

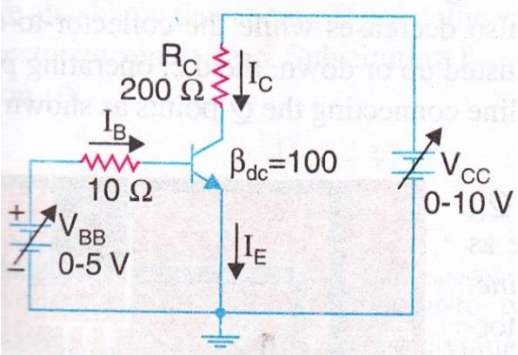
a) Explain the concept of DC load line used in BJT amplifier.

Ans:

Concept of DC load line:- **01M**

For proper operation of a transistor a fixed level of certain currents and voltage in a transistor are set. These values of current and voltage defines the point at which the transistor operates this point is called operating point. It is also known as quiescent point or simply Q-point.

Explanation with Diagram:- **03M**



Consider the transistor circuit shown in the fig. for this circuit we know that the value of collector current is given by the relation.

$$I_C = \frac{V_{CC} - V_{CE}}{R_C}$$ .....Equation (i)

Where,

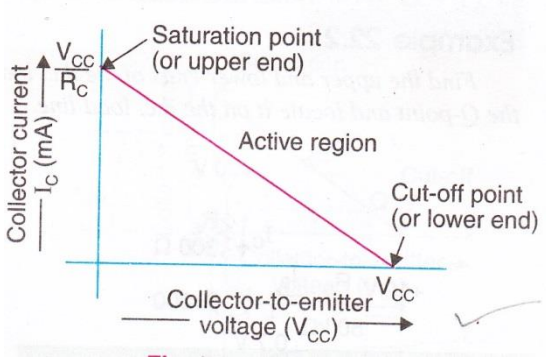
V_{CC} = Value of DC supply voltage in the collector circuit.

V_{CE} = The value of collector to emitter voltage and

R_c = value of collector resistance

The value of collector to emitter voltage (V_{CE}) at saturation point is very small as compare to V_{CC} supply. Therefore

$$I_C = \frac{V_{CC}}{R_C}$$



At cut off point the value of collector current is zero substituting $I_C = 0$ in equation (i)

$$0 = \frac{V_{CC} - V_{CE}}{R_C}$$

OR

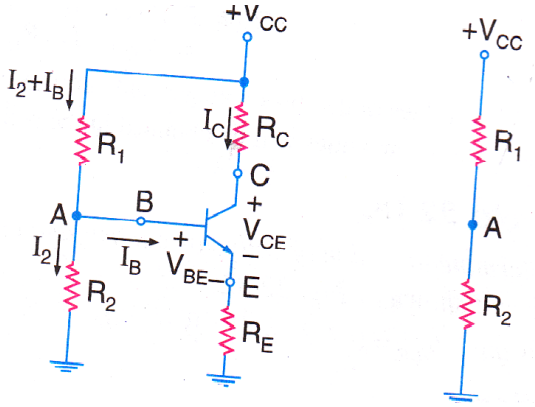
$V_{CE} = V_{CC} = V_{CE(cut\ off)}$……..Equation (ii)

Equation (i),(ii) are the Q point coordinate of DC load line.

b) Draw the circuit diagram of voltage divider biasing circuit used with BJT CE amplifier and explain its operation.

Ans:

Diagram:- **02M**



Explanation:- **02M**

In all the D.C. bias circuits, the value of D.C. bias current and voltage of the collector depends upon the current gain (β) of the transistor. But we know that the value of current gain (β) is temperature sensitive, therefore it would be desirable to provide a D.C. bias circuit which is independent of the transistor current gain (β). It is commonly known as voltage divider bias or self-bias circuit

The name voltage divider is derived from the fact that resistor R_1 and R_2 form a potential divider across the V_{CC} supply. The voltage drop across resistor R_2 forward biases the base – emitter junction of a transistor. The emitter resistor (R_E) provides the D.C. stability.

It is evident from that the voltage at the transistor base (due to the voltage divider network of resistors R_1 and R_2).

$$V_B = V_{CC} x \frac{R_2}{R_1+R_2}$$

Since the voltage drop across the base – emitter junction (V_{BE}) when forward biased is very small, as compared to the voltage at the base (V_B), therefore the voltage at the emitter is almost equal to the voltage at the base i.e. ., Neglecting V_{BE}

Therefore value of emitter current,

$$I_E = \frac{V_E}{R_E}$$

And the value of collector current,

$$I_C = I_E$$

The voltage drop across the collector resistor,

$$V_{RC} = I_C * R_C$$

And the voltage at the collector (measured with respect to the ground)

$$V_C = V_{CC} - V_{RC} = V_{CC} – I_C * R_C$$

The voltage from collector – to – emitter.

$$V_{CE} = V_C – V_E = V_{CC} – I_C * R_E$$

$$V_{CE} = V_{CC} – I_E(R_C + R_E) \ldots\ldots\ldots\ldots\ldots\ldots (I_C = I_E)$$

c) Draw the constructional sketch of n channel JFET and explain its working principle

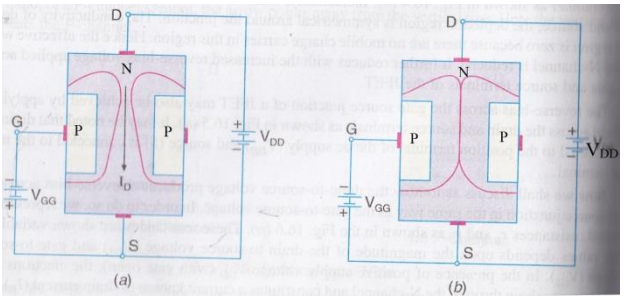
Ans:-

Working Principle: **02M**

- When a voltage V_{DS} is applied between drain and source terminal and voltage on the gate is zero, the two PN junctions at the sides of the bar produce depletion layers.
- The electrons will flow from source to drain through a channel between the depletion layers. The size of these layers determines the width of the channel and hence the current conduction through the bar.

- When a reverse voltage V_{GS} is applied between the gate to source in figure (2) the width of the depletion layers is increased.
- This reduces the width of conducting channel thereby increasing the resistance of n type bar consequently the current from the source to drain is decreased.
- Hence current from source to drain can be controlled by the application of potential (i.e. electric field) on the gate for this reason the device is called as field effect transistor (FET).

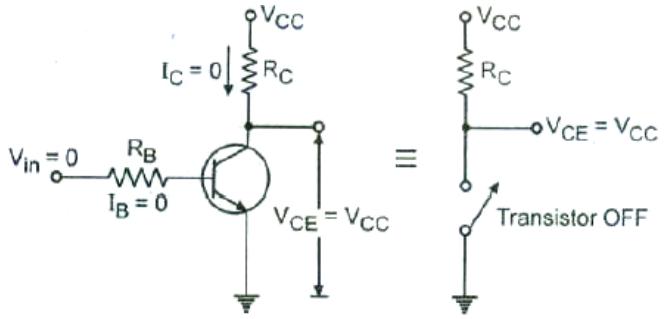
Diagram:- **02M**



d) With neat circuit and waveform diagram explain how BJT works as switch

Ans:-

Diagram: **2M**



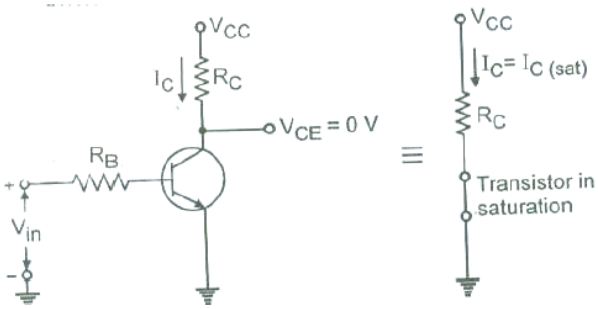
Working: **2M**

The transistor can be used for two types of application viz. amplification and switching. For the amplification as a transistor is biased in its active region. Whereas for switching applications it is biased to operate in the saturation (full ON) or cut off (full OFF) region.

a. Transistor in cut- off region (open switch):

- In the cut –off region both the junction of a transistor are reverse biased and very small reverse current flows through the transistors.
- The voltage drop across the transistor (V_{CE}) is high. Thus, in the cut off region the transistor is equivalent to an open switch as shown in figure.

b. Transistor in the saturation region (Closed switch):

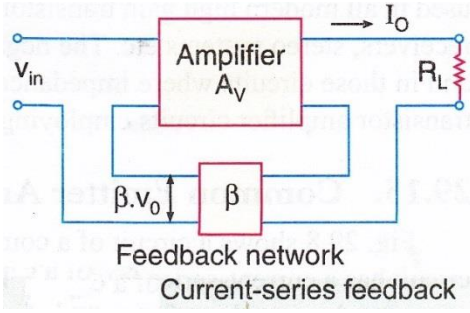


- When Vin is positive a large base current flows and transistor saturates.
- In the saturation region both the junctions of a transistor are forward biased. The voltage drop across the transistor (V_{CE}) is very small, of the order of 0.2 V to 1V depending on the type of transistor and collector current is very large.
- In saturation the transistor is equivalent to a closed switch.

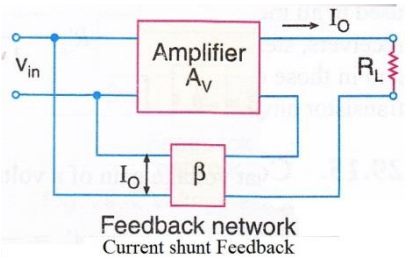
e) Draw the block diagram of current series and current shunt feedback.

Ans:-

Current Series Feedback:- **02M**



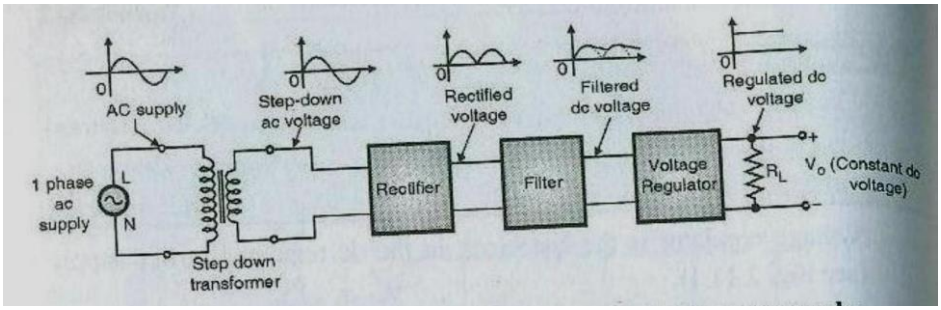
Current Shunt Feedback:- **02M**



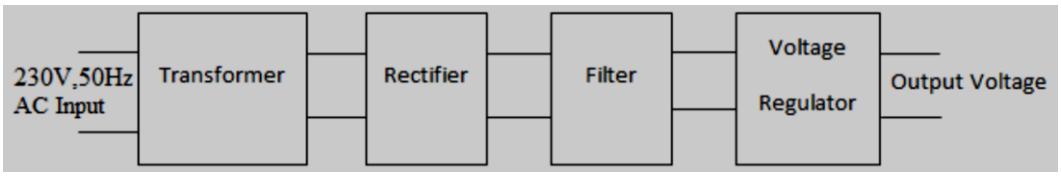
f) Draw the block diagram of DC regulated power supply and State the function of each block.

Ans:-

Diagram: **02M**



OR



Functions of each block: **02M**

Step Down Transformer

A step down transformer will step down the voltage from the ac mains to the required voltage level. The output of the transformer is given as an input to the rectifier circuit.

Rectification

Rectifier converts an alternating voltage or current into corresponding pulsating dc .Usually a full wave rectifier or a bridge rectifier is used to rectify both the half cycles of the ac supply.

DC Filter

The rectified voltage from the rectifier is a pulsating dc voltage having very high ripple content. Hence a filter is used. Different types of filters are used such as capacitor filter, LC filter, Choke input filter, π type filter.

Regulator

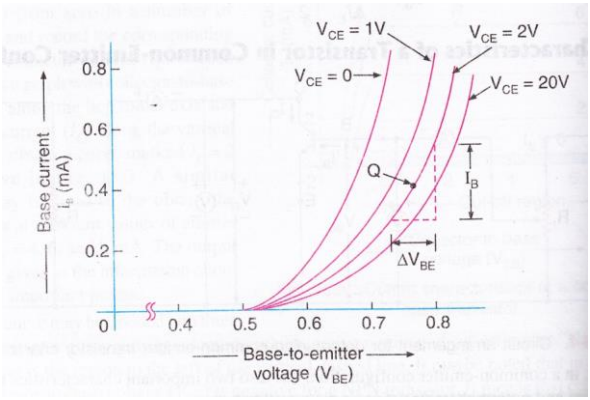
The output voltage or current will change or fluctuate when there is change in the input from ac mains or due to change in load current at the output of the regulated power supply or due to other factors like temperature changes. This problem can be eliminated by using a regulator. A regulator will maintain the output constant even when changes at the input or any other changes occur.

Q3 Attempt any four **16M**

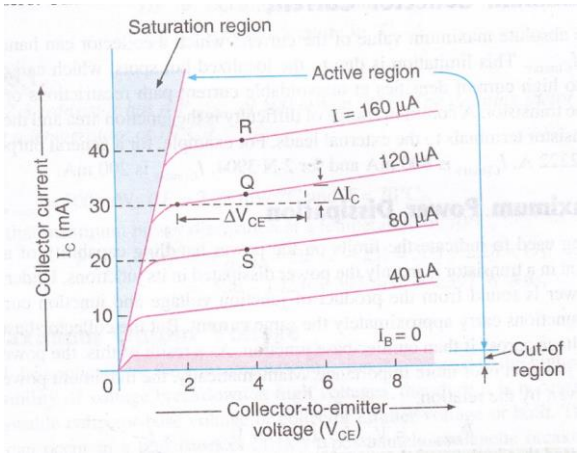
a) Draw the input and output characteristics of CE configuration and label it.

Ans:

Input Characteristic of CE configuration: **02M**



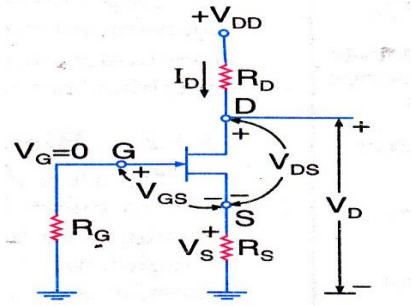
Output Characteristics of CE configuration: **02M**



b) With neat circuit diagram and mathematical expression explain the self-biasing used in FET.

Ans:

Circuit Diagram: - **02M**



Explanation and mathematical Expression:- **02M**

- It is most common type of JFET bias.
- JFET must be operated such that the VGS is always Reverse Biased.
- This condition requires a –ve VGS for N-channel JFET and +ve VGS for p-channel JFET.
- This can be achieved using the self-bias arrangement.
- The gate resistor R_G does not affect the bias because it has essentially no voltage drop across it and therefore the gate remains at 0V.
- R_G is necessary only to isolate and as signal from ground in amplifier application.
- Is produces a voltage drop across R_S and makes source +Ve with respect to ground

$$Is=I_D \ \& \ V_G=0$$

$$V_S=I_DR_S$$

The gate to source voltage is

$$V_{GS}=V_G-V_S$$

$$=0-I_DR_S$$

$$\text{Therefore} \quad V_{GS}=-I_DR_S$$

For p- channel, the current through R_S produces a – Ve voltage at source making gate +Ve with respect to source.

$$I_S=I_D$$

$$V_{GS}=+I_D*R_S$$

The drain voltage with respect to ground is given as ,

$$V_D=V_{DD}-I_DR_D$$

Since $V_S=I_D*R_S$ the drain to source voltage

$$V_{DS}=V_D-V_S$$

$$=V_{DD}-I_DR_D-I_DR_S$$

$$V_{DS}=V_{DD}-I_D(R_D+R_S)$$

Setting the Q-point of self-biased JFET:

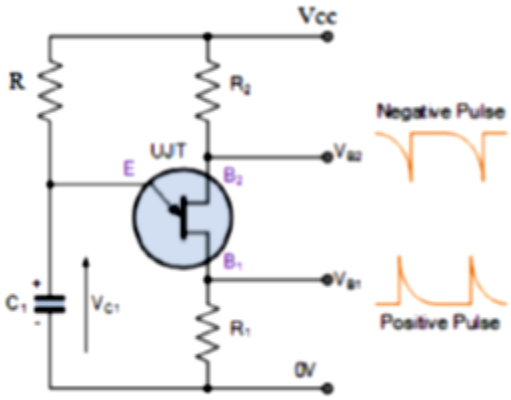
The basic approach to set a JFET Bias point is to determine I_D for a desired value of V_{GS} or Vice-Versa. Then calculate the required value of R_S using relation of

$$R_S=\left|\frac{V_{GS}}{I_D}\right|$$

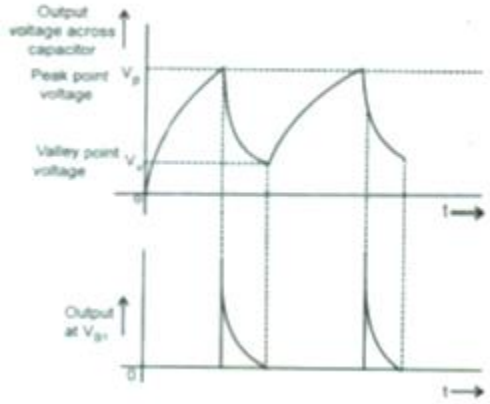
c) Draw the circuit diagram and explain the working principle of UJT relaxation oscillator.

Ans: -

Circuit diagram:- **01M**



Waveform: **01M**



Working principle: - **02M**

- When the supply voltage (V_{CC}) is switched ON, the capacitor charges through resistor (R), till the capacitor voltage reaches the voltage level (V_P) which is called as peak point voltage. At this voltage the UJT turns ON.
- As a result of this, the capacitor (C) discharges rapidly through resistor (R_1). When that capacitor voltage drops to level Vv (called valley- point voltage) the uni-junction transistor switches OFF allowing the capacitor (C) to charge again.
- In this way because of the charging and discharging of capacitor the exponential sweep voltage will be obtained at the emitter terminal of UJT. The voltage developed at base 1(V_{B1}) terminal is in the form of narrow pulses commonly known as trigger pulses.
- The sweep period depends upon time constant (R.C) and the sweep frequency can be varied by changing value of either resistance (R) or capacitor (C). Due to this fact, the resistor R is shown as a variable resistor.
- The sweep period is given by the relation

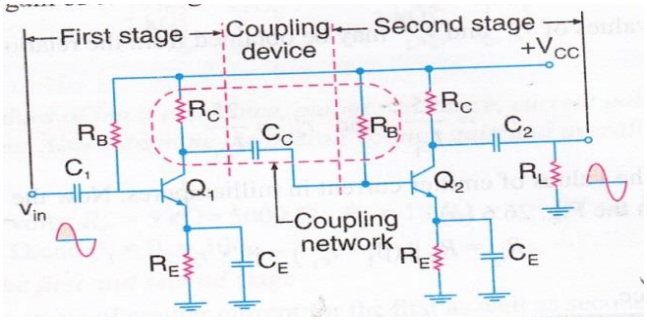
$$T = R.C. \log_e (1/1-n)$$

$T = 2/3\ R.C.\ \log_{10}(1/1-n)$

d) Draw the circuit diagram and frequency response of two stage RC coupled amplifier and explain its operation. State its important characteristics.

Ans: ***Note: (Circuit Diagram may be drawn with voltage divider biasing)***

Circuit diagram RC coupled amplifier : - **01M**



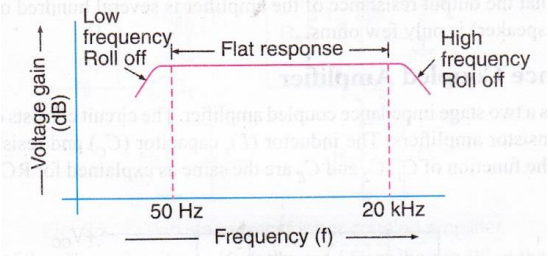
- This is the popular type of coupling method. It is usually employed for voltage amplification following fig shows two stage of an RC coupled amplifier.
- A coupling capacitor C_c is used to connect the output of first stage to the base of the second stage and so on.
- The resistance R_1, R_2 and R_E form the biasing and stabilization network. The emitter bypass capacitor offers low reactance path to the signal. The coupling capacitor C_E transmits ac signal but blocks dc. This prevents dc interference between various stages and the shifting of Q-operating point.

Operation: - **01M**

- When ac signal is applied to the base of the first transistor, it appears in the amplified form across its collector load R_C is given to base of next stage through coupling capacitor Cc.
- The second stage does further amplification of the signal. In this way the cascaded (in series) stage will amplify the signal further and overall gain is considerably increased.

Frequency response:- **01M**

Following fig. shows frequency response of typical RC coupled amplifier.



From above frequency it is clear that bandwidth of RC coupled amplifier is large. Voltage gain drops off at low (50Hz) and high (20Hz) frequencies. Whereas it is uniform over mid frequency range.(50Hz, to 20KHz).

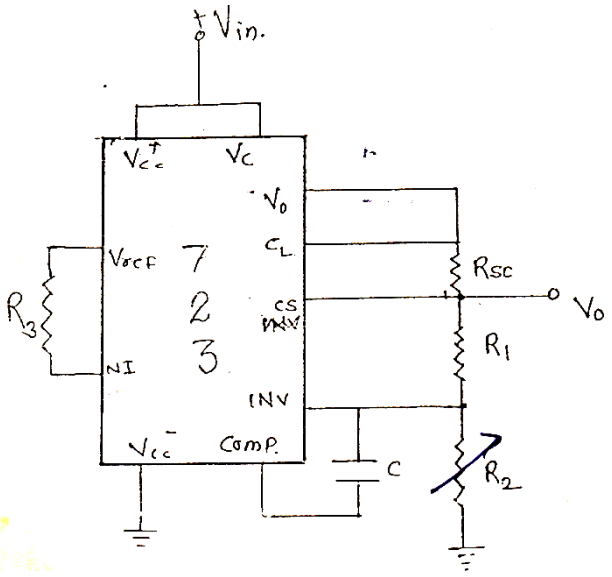
Application:- (Any one) **01M**

- RC coupled amplifier is used as a voltage amplifier.
- In PA system.

e) Draw the high voltage regulated using IC 723 and Explain its operation.

Ans:-

Diagram:- **02M**



Explanation: - **02M**

This circuits is basically used for 7V to achieve this a potential divider is connected between actual terminal V_0 and ground .and the voltage at NI terminal of the error amplifier is Vref

$$V_{NI}=V_{ref}$$

The voltage at the INV terminal of the error amplifier due to R_1, R_2 divider is

2)

The difference of error amplifier

That is,

$$V_{ref} - V_{out}\left(\frac{R_2}{R_1+R_2}\right) = 0$$

$$V_{ref} = V_{out}\left(\frac{R_2}{R_1+R_2}\right)$$

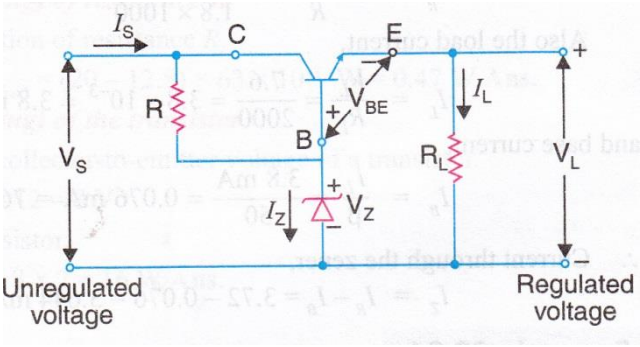
$$V_{out} = V_{ref}\left(\frac{R_1+R_2}{R_2}\right)$$

$$\boxed{V_{out} = V_{ref}\left(1+\frac{R_1}{R_2}\right)}$$

f) Draw the circuit diagram of transistorized series voltage regulator and explain its working. State its advantage and disadvantages.

Ans:-

Circuit Diagram:- **01M**



Above fig shows a circuit of a transistorized series regulator. Since the transistor is connected in series with the load, therefore this circuit is known as a series voltage regulator.

Operation:- **01M**

The unregulated DC supply is fed to the input terminal as shown in above fig.

- The output voltage is given by

$$V_L = V_Z - V_{BE}$$

- V_Z being a zener voltage is assumed to be a constant therefore if the output voltage varies, and then there will be a change in V_{BE}.
- If the output voltage increases due to some reason then V_{BE} decreases and due to this base current decreases. Therefore collector current decreases.
- This will increase the collector to emitter voltage (V_{CE}) across the transistor and V_L will be regulated.

$V_L = Vs - V_{CE}$.

- If the output voltage decreases then exactly opposite action will takes place and the output voltage is regulated.
- The circuit's action may be summarized in the form of the following equation.

$$V_L\downarrow \rightarrow V_{BE}\downarrow \rightarrow I_B\downarrow \rightarrow I_C\downarrow \rightarrow V_{CE}\uparrow \rightarrow V_L\downarrow.$$

Advantages :- (Any two) **½ M each**

- Voltage regulation is better than shunt regulation.
- Transistor is used as emitter follower hence R_o is very low .
- Less ripple contain in the output because of negative feedback.

Disadvantage:- (Any two) **½ M each**

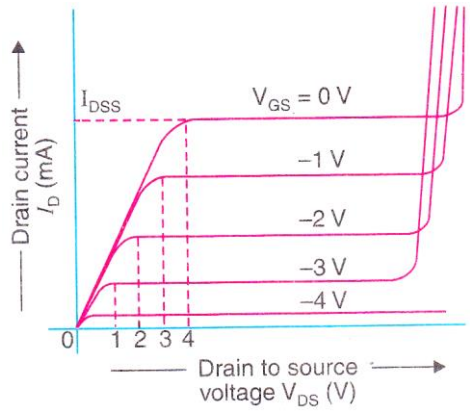
- V_o is not adjustable.
- Large power dissipation in series transistor.
- Heats sink is required for transistor which increases the cost.
- No protection for transistor against accidental short circuits of terminal.

Q.4 Attempt any four **16M**

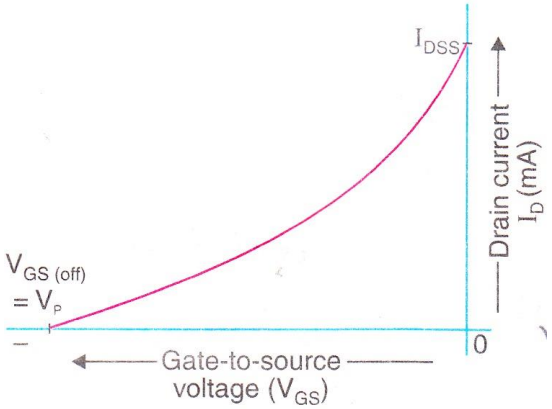
a) Draw the drain characteristics and transfer characteristics of JFET.

Ans:-

Drain characteristics: - **02M**



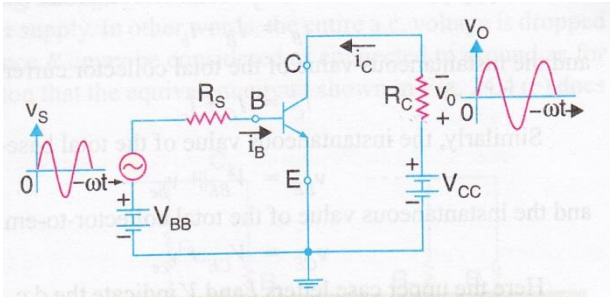
Transfer characteristics:- **02M**



b) How BJT can be used as an amplifier? Explain.

Ans:-

Circuit Diagram:- **02M**



Explanation:- **02M**

- If for a small change in input voltage, a proportional large change in output voltage is obtained.
- The transistor is operated in the CE configuration the output voltage V_0 is taken at the collector with respect to ground

$$V_0=V_{CE}$$

- Due to small change in ΔVin, there will be a small change in I_B

$$\Delta I_B=\frac{\Delta V_{in}}{R_B}$$

- Hence the corresponding change in collector current is given by

$$\Delta I_C=\beta I_B$$

Hence the corresponding change output voltage is given by

$$\Delta V_0=I_C*R_C$$

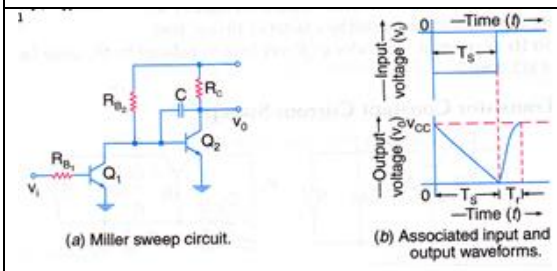
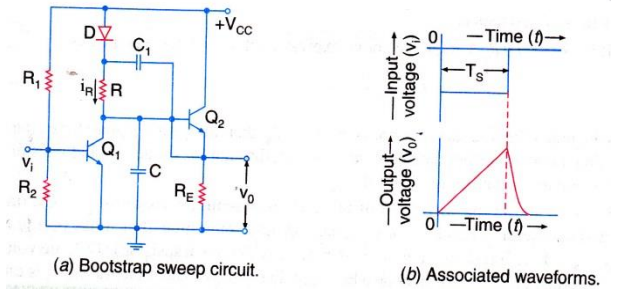
$$=\beta*\frac{\Delta V_{in}}{R_B}*R_C$$

as R_B, R_C, β are constants HenceΔV_0 is directly proportional to ΔV_{in}

Thus for a small change in Vin we get a large change in V_0 and voltage amplification takes place. Hence the BJT acts as a voltage amplifier.

c) Compare miller integrator and bootstrap sweep generator with respect to the technique used.

Ans:-

Miller Integrator	Bootstrap sweep generator
• In this method as OPAMP based integrator is used to convert a step into a ramp waveform. **½ M**	• In this method a constant current is approximated by maintaining nearly constant voltage across a fixed resistor in series with a capacitor. **½ M**
 (a) Miller sweep circuit. (b) Associated input and output waveforms. **01M**	 (a) Bootstrap sweep circuit. (b) Associated waveforms. **01M**
• The rate of decrease of output voltage is controlled by the rate of discharge of capacitor. The time constant of discharge is very large hence practically discharge current remains constant. **½ M**	• Capacitor 'C' charged with a constant current which causes the voltage across capacitor 'C' to increase linearly with time .The CKT pulls itself up by its own bootstrap. **½ M**

d) Compare small signal amplifier and power amplifier (Any 4 points)

Ans:-

Any four point **1M each**

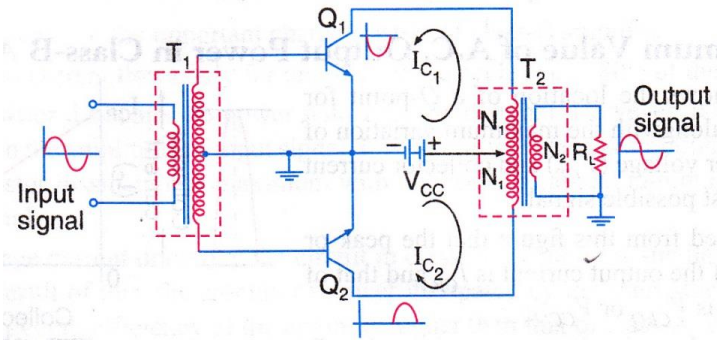
Sr No.	Small Signal Amplifier/ voltage amplifier	Power Amplifier
1	Transistor used in voltage amplifier has a large value of current gain (β) is nearly 100 as compare to that of power amplifier.	Transistor used in power amplifier has current between 20& 50.
2	The input voltage to base of transistor in voltage amplifier is low (a Few mV).	The input voltage to base of transistor in power amplifier is high (2-4 V)
3	Input resistance is quite low as compare to output resistance.	Input resistance is very large as compared to output resistance
4	The physical size of the transistor used in voltage amplifier is used in voltage small known as low or medium power transistor.	Power amplifier uses larger size transistors.

5	Voltage amplifier uses RC coupling for interstate connection.	Power amplifier uses transformer coupling.

e) Draw the circuit diagram of class-B push-pull amplifier and explain its operation. State its important applications.

Ans:

Circuit Diagram:- **02M**



Operation :- **01M**

- In class B amplifier transistor conduct only for half cycle of input signal.one conduct in positive half cycle and other conducts in negative half cycle.
- Transformer T_1 is called as input transformer called phase splitter and produces two signals which are 180 degree out of phase with each other.
- Transformer T_2 is called as output transformer and is required to couple the a.c signal from the collector to the load.
- When there is no input signal both the transistor Q_1 and Q_2 are cut off hence no current is drawn from V_{cc} supply. Thus there is no power wasted in stand by the power dissipation in both transistor is practically zero.
- During positive half cycle Q_1 ON Q_2 OFF and at the output half cycle is obtained during negative half cycle Q_1 OFF and Q_2 on hence another half cycle is obtained at the output.
- Then output transformer joins these two halves and produces a full sine wave in the load resistor.

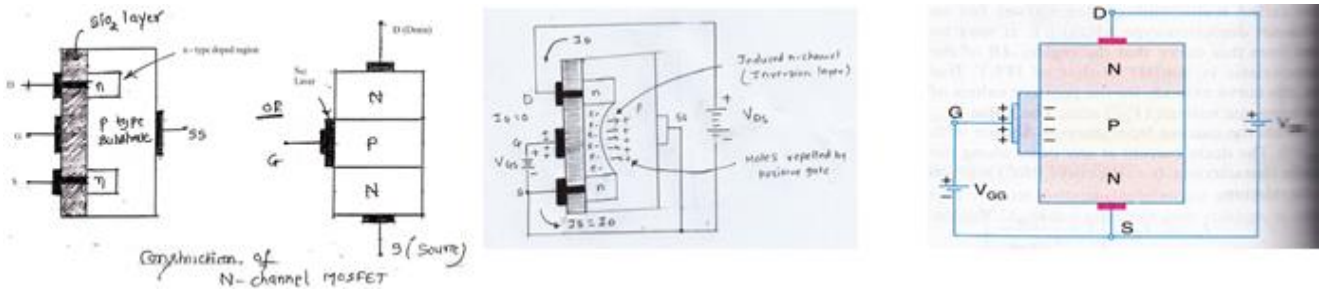
Application:- **01M**

- This amplifier is frequency employed in the output (or final) stages of the amplifier circuits.
- These are used in public address systems (PAS's) tape recorders and stereo amplifiers.

f) With neat sketch explain working principle of enhancement type MOSFET. State its important applications.

Ans:-

Diagram:- **02M**



Working principle:- **01M**

Case1:- When V_{GS}=0 volt

If V_{GS}=0 volt and a +ve voltage applied between its drain and source, then due to the absence of the n-type channel a zero drain current will result.

Case2:- When V_{GS}=positive and V_{GS}=positive

- The +ve potential at the gate terminal will repel the holes present in the p-type substrate.
- This results in creation of a depletion region sio_2 insulting layer. But the minority carriers i.e the e-s in the p-type substrate will be attracted towards the gate terminal and gather near the surface of sio_2 layer.
- As we increase the positive V_{GS}, the number of electrons gathers near Sio_2 layer we increase.
    - The electron concentration near Sio_2 layer increase to such an extent that it creates an induced n-channel. This connects the n-type doped region. This induced n-channel is called 'inversion layer'. The drain current then start flowing through this induced channel. And the value of V_{GS} at which this conduction begins is called as 'threshold voltage' $V_{GS\ (TH)}$.

Case 3:- Effect of increasing in V_{DS}

- The $+V_{GS}$ is kept constant and the V_{GS} is increased gradually .due to this, the gate terminal becomes less and less +ve with respect to drain. So less number of electrons are attracted towards gate terminal and the induced channel becomes narrow that means, the channel width will be reduced to a point of pinch off and the saturation condition will occur, hence I_D will remains constant.

Application:- **½ Mark each**

- As an amplifier.
- As a switch.

Q5 Attempt any four: **16M**

a) Define α, β and γ w.r.t BJT. Derive the relation between α andβ.

Ans:-

Definitions : **02M**

α_{dc} is defined as the ratio of collector current I_C to the emitter current I_E

$$\alpha_{dc} = I_C / I_E$$

- β_{dc} is defined as the ratio of collector current I_C to the Base Current I_B

$$\beta_{dc} = I_C / I_B$$

- γ_{dc} is defined as the ratio of emitter current I_E to the Base Current I_B

$$\gamma_{dc} = I_E / I_B$$

Relation between α and β: **02M**

$$\beta = \frac{\Delta IC}{\Delta IB} \quad \text{---------- (i)}$$

$$\alpha = \frac{\Delta IC}{\Delta IE} \quad \text{---------- (ii)}$$

Now $I_E = I_B + I_C$

Or $\Delta I_E = \Delta IB + \Delta IC$

Or $\Delta I_B = \Delta IE - \Delta IC$

Substituting the value of ΔIB in exp (i), we get

$$\beta = \frac{\Delta IC}{\Delta IE - \Delta IC}$$

Dividing the numerator and denominator of R.H.S of exp. (iii) by Δ IE, we get

$$\beta = \frac{\Delta IC / \Delta IE}{\frac{\Delta IE}{\Delta IE} - \frac{\Delta IC}{\Delta IE}}$$

$$= \frac{\alpha}{1-\alpha} \quad \text{----------Since } [\alpha = \frac{\Delta IC}{\Delta IE}]$$

$$\beta = \frac{\alpha}{1-\alpha}$$

OR

$$\alpha = \frac{\Delta IC}{\Delta IE}$$

$$\alpha = \frac{\Delta IC}{\Delta IB + \Delta IC}$$

$$\frac{\Delta IB + \Delta IC}{\Delta IC} = \frac{1}{\alpha}$$

$$\frac{\Delta IB}{\Delta IC} + \frac{\Delta IC}{\Delta IC} = \frac{1}{\alpha}$$

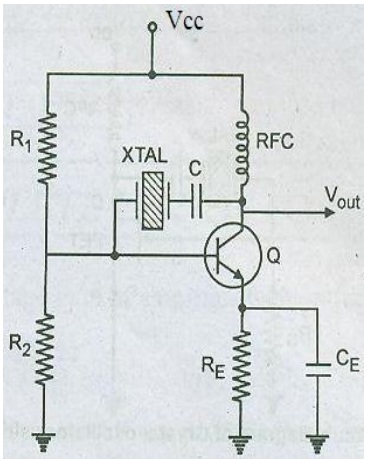
$$\frac{1}{\beta} + 1 = \frac{1}{\alpha}$$

$$\alpha = \frac{\beta}{1+\beta}$$

b) State the working principle of crystal oscillator and list its two applications.

Ans:-

Circuit Diagram:- **01½M**



Working Principle of Piezoelectric Crystal: **01½M**

- A Quartz Crystal has a very peculiar property known as Piezoelectric Effect.
- According to this effect, when an AC voltage is applied across a quartz crystal, it vibrates at a frequency of applied voltage.
- Conversely, if a mechanical force is applied to vibrate a quartz crystal it generates an AC voltage.
- Above fig shows the circuit of crystal oscillator using transistor. In this circuit, the crystal is connected as a series element in the feedback path from collector to the base.
- The resistors R_1, R_2 and R_E provide voltage divider stabilized d.c. bias circuit. The capacitor C_E provides a.c bypass of emitter resistor and RFC coil provides for d.c bias. The coupling capacitor C has negligible impedance at the circuit operating frequency.
- The circuit frequency of oscillation is set by the series resonant frequency of the crystal and its value is given by the relation

$$F = \frac{1}{2\pi\sqrt{LC}}$$

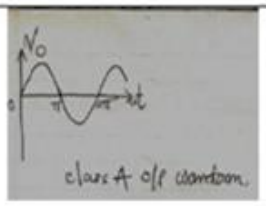
Applications crystal oscillator (any two points) **½M each**

1. In the radio and TV transmitters.
2. In Special type receivers.
3. As a crystal clock in microprocessors.
4. In the frequency synthesizers.

c) Compare class A, class B and class AB power amplifiers (Any four points)

Ans: **01Meach**

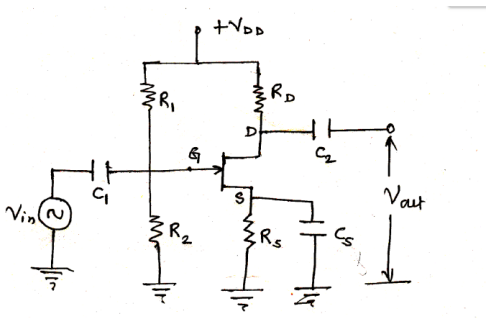
Note:Marks should be given to other valid parameters

Parameter	Class A	Class B	Class AB
Position of operating pt. on load line	Q point is at the centre of load line.	On X axis	Just above X axis.
efficiency	lowest efficiency 25% to 50%	Above 78.5%	Between 50 to 78.5%
Conduction Angle	Conducts for (360^0) full cycle of input signal	(180^0) half cycle of input signal.	Greater than 180^0 and less than 360^0
O/P waveform			

d) Draw the circuit diagram common source FET amplifier and explain its working principle. State its applications.

Ans:

Circuit Diagram:- **02M**



Common Source FET amplifier

Operation: **01M**

- When small a.c. signal is applied to the gate, its produces variation in the gate to source voltage. This produces variation in the drain current. As the gate to source voltage increases the current also increases. As the result of this voltage drop across R_D also increases. This causes the drain voltage to decreases.
- In positive half cycle of the input ac signal the gate to source voltage becomes less negative. This will increase the channel width and increase the level of drain current I_D. Thus I_D vary sinusoidally above its Q point value.
- The drain to source voltage V_{DS} is given by $V_{DS} = V_{DD} – I_D R_D$
- Therefore as I_D increases the voltage drop $I_D R_D$ will also increase and voltage V_{DS} will decrease.
- If ΔI_D is large for a small value of ΔV_{GS} , the ΔV_{DS} will also be large and we get amplification. Thus the AC
- Output voltage V_{DS} is 180º out of phase with AC input voltage.

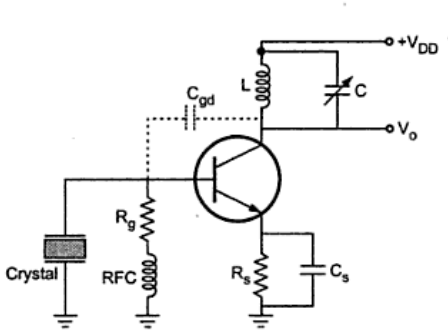
Applications : (Any two) **½M each**

1. In radio and TV amplifier circuit.
2. In PA system.
3. As a voltage amplifier.
4. As a pre amplifier in audio circuits

e) Draw the circuit diagram of Miller crystal oscillator and explain its operation. State advantages and disadvantages of crystal oscillator.

Ans: ***Note: any relevant circuit diagram can be considered***

Circuit Diagram: **02M**



Working: **01M**

- The Hartley oscillator circuit can be modified to get miller crystal oscillator. In Hartley oscillator circuit, two inductors and one capacitor is required in the tank circuit. One inductor is replaced by a crystal which acts as a

inductor for the frequencies greater than the series resonant frequency. The transistorized Miller crystal oscillator is shown in the figure.

- The tuned circuit L and C is off tuned to behave as an inductor ie. L_1. The crystal behaves as other inductance L_2 between base and ground. The internal capacitance of the transistor acts as a capacitor required to fulfill the elements of the tank circuit. The crystal decides the operating principle of the oscillator.

Advantages: (Any one) **½M**

1. Very high frequency stability.
2. The Q is very high.
3. It is possible to obtain very high, precise and stable frequency of oscillations.
4. Very low frequency drifts due to change in temperature and other parameters.

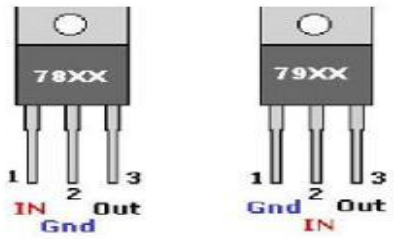
Disadvantages: **(Any one)** **½M**

1. Crystal of low fundamental frequencies are not easily available.
2. These are suitable for high frequencies applications.

f) Draw the pin diagram of IC 78XX and IC79XX and state their features and advantages.

Ans:

Pin Diagram: **02M**



Features: (Any Two) **½ M each**

1. Programmable output.
2. Facility to boost the voltage/current.
3. Internally provided short circuit current limiting.
4. Thermal Shutdown.
5. Floating operation to facilitate higher voltage output.
6. Versatility and low cost.
7. They are easy to use.

Advantages: (Any One) **01M**

- 78xx and 79xx series ICs do not require additional components to provide a constant, regulated source of power, making them easy to use, as well as economical and efficient uses of space.
- 78xx and 79xx series ICs have built-in protection against a circuit drawing too much current. They have protection against overheating and short-circuits, making them quite robust in most applications.

Q6. Attempt any four: **16M**

a) What do you understand by stabilization of operating point? Explain the need for stabilization.

Ans:

Meaning of stabilization: **02M**

- The process of making operating point independent of temperature changes or variation in transistor parameter is known as stabilization.
- The maintenance of the operating point stable is called the stabilization.

Need for stabilization: **02M**

The stabilization of operating point is essential because of:

- **Temperature dependence of I_C**

  With the increase in temperature, the collector leakage current I_{CO}, the current gain ß tend to increase and V_{BE} required to produce a given collector current I_C tends to decrease. Thus increase in temperature tends to cause increase in I_C.

- **Individual variations**

  The value of ß and V_{BE} are not exactly the same for any two transistors even of the same type. So when a transistor is replaced by another one (even of the same type) the operating point (zero signals I_C and V_{CE}) is shifted.

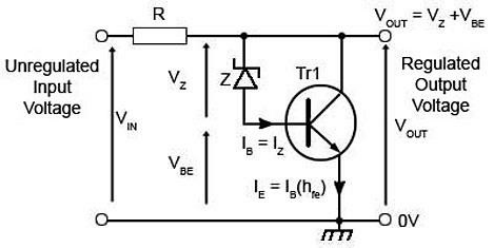
- **Thermal runaway**

  The collector current I_C, being equal to $ßI_B + (1+ ß) I_{CO}$, increases with the increase in temperature. This leads to increased power dissipation with further increase in temperature. Being a cumulative process, it can lead to thermal runaway resulting in burn out of the transistor.

b) Draw the diagram transistorized shunt regulator and explain its working.

Ans:

Circuit Diagram: **02M**



Working: **02M**

- From the above circuit the load voltage is given by
- $V_L = V_Z + V_{BE}$ Or $V_{BE} = V_L - V_Z$ …… (i)
- Since the load voltage for a given zener diode is fixed, therefore any decrease or increase in load voltage will have a corresponding effect on the base to emitter voltage V_{BE}.
- The unregulated input voltage increases, load voltage also increases. As a result of this from equation (i) above, we find that V_{BE} is also increases. And the base current I_B increases. Due to this the collector current I_C also increases. This causes the input current (I_S) to increase, which in turn increases the voltage drop across series resistance (V_{RS}) . Consequently, the load voltage decreases.
- If the output voltage decreases then V_{BE} will decrease. This will reduce the collector current Ic. So more current will flow through the load and the load voltage will increase. This increase in load voltage will compensate the initial decrease in load voltage. Thus output voltage gets regulated.

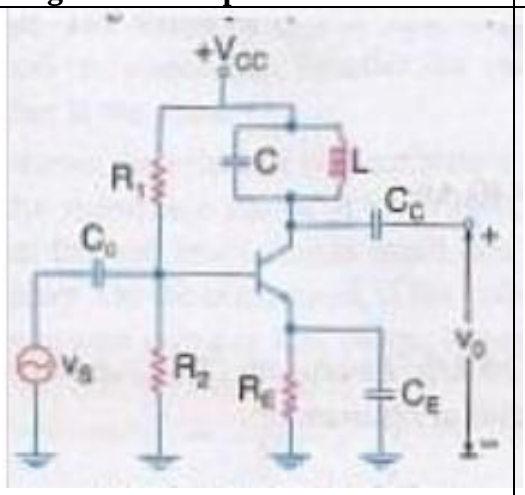
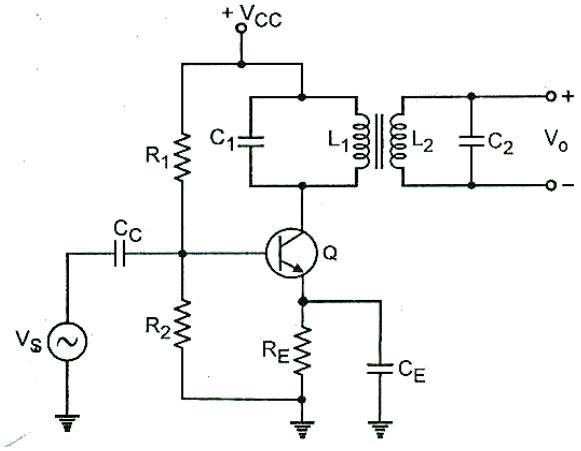
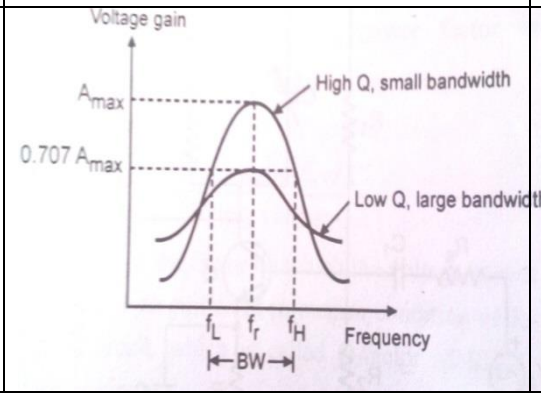
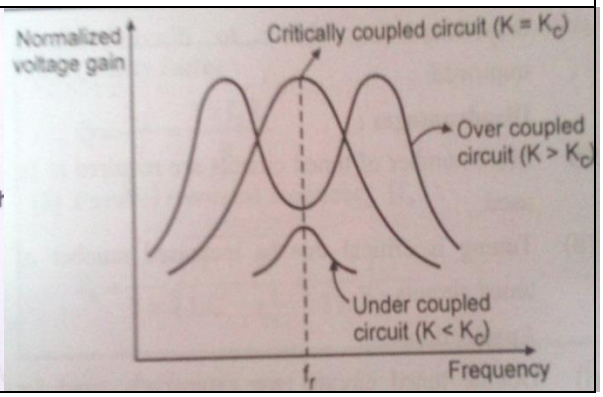
c) Compare positive feedback and negative feedback (any four points).

Ans: (Any four points): **01M each**

Sr. No.	Parameter	Positive feedback	Negative Feedback
1.	Overall Phase shift	0◦ or 360◦	180◦
2.	Input voltage	Increases	Decreases
3.	Output voltage	Increases	Decreases
4.	Feedback signal and input signal	Are in phase	Are out of phase
5.	Voltage gain	Increases	Decreases
6.	Noise	Increases	Decreases
7.	Bandwidth	Decreases	Increases
8.	Application	Oscillators, Schmitt triggers	Amplifier

d) Compare single tuned amplifier and double tuned amplifier w.r.t circuit diagram and frequency response.

Ans: **02M each**

Parameter	Single tuned amplifier	Double tuned amplifier
Circuit diagram		
Frequency Response		

e) What do you mean by an oscillator? State Barkhausen's criteria required for oscillations. State important application of oscillator.

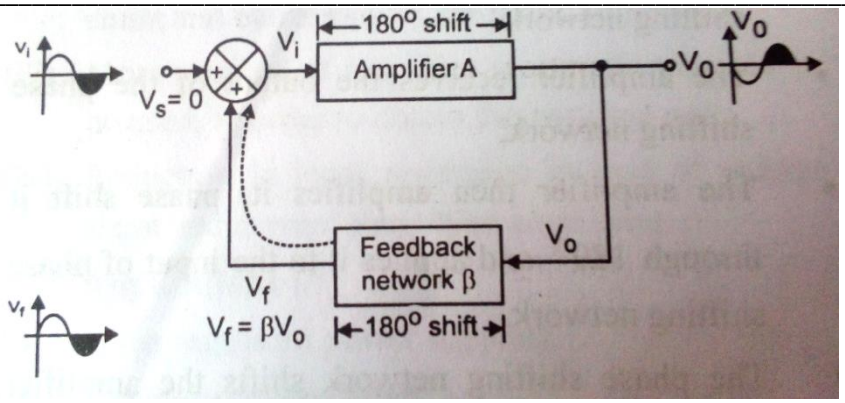
Ans:

Oscillator: **01M**

Oscillator is basically ac signal generators which you use in your laboratories. Oscillators generate alternating voltage of desired shape at desired frequency. Oscillators work on the principle of positive feedback.

Barkhausen's Criteria: **02M**

(Note: Diagram is optional)



An amplifier will work as an oscillator if and only if it satisfies a set of conditions called Barkhausen's criterion.

It states that:

- An oscillator will operate at that frequency for which the total phase shift around loop equals to 0◦ or 360◦.
- At the oscillator frequency, the magnitude of the product of open loop gain of the amplifier A and the feedback factor β is equal or greater than unity.

ie. $A\beta \geq 1$

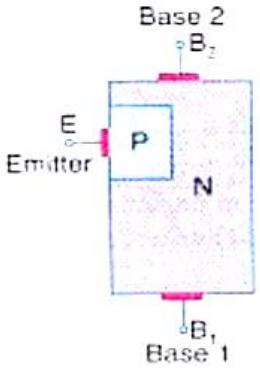
Applications of Oscillator: **(Any one)** **01M**

1. Low and medium sine wave generators.
2. In the radio and TV transmitters.
3. In frequency synthesizers.
4. In special type of receivers.

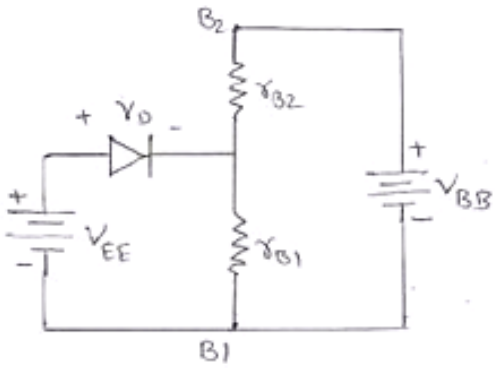
f) Draw the constructional sketch and equivalent circuit of UJT and explain its V-I characteristics.

Ans:

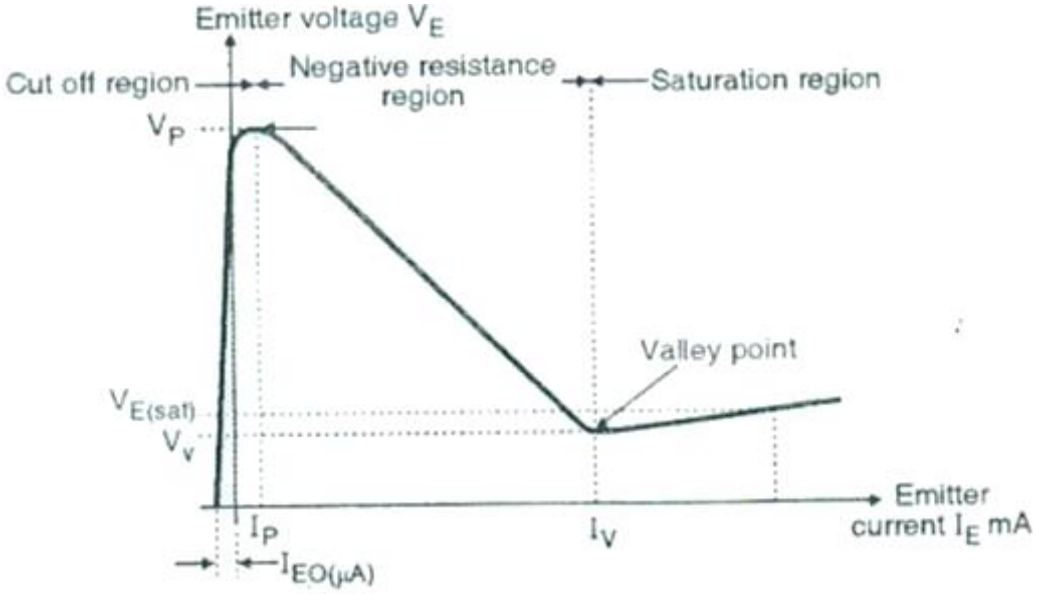
Construction: **01M**



Equivalent Diagram: **01M**



V-I Characteristic and explanation : **02M**



- This is graphically representation of emitter voltage versus emitter current. For the emitter potentials less than Vp the UJT is in OFF state.
- As emitter potential increases and reaches $Vp = \eta V_{BB} + V_D$, the UJT starts conducting. Then with increase in emitter current I_E the emitter voltage decreases.
- The reduction in voltage across UJT is due to the drop in resistance R_{B1} With increase in value of I_E.
- This region is known as "Negative Resistance" region, which is stable enough to be used in various applications.
- Eventually valley point will be reached and a further increase in I_E will place the device into saturation.